APPLICATION NOTE

TEMPCO and VDDC_LV Power Reduction Optimization (PRO)

Ultra-Low Power Apollo4 Plus SoC Family

A-SOCA4P-ANGA01EN v1.0

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Revision History

Revision	Date	Description
1.0	December 7, 2022	Initial Release.

Reference Documents

Document ID	Description
DS-A4P-x	Apollo4 Plus Datasheet
DS-A4BP-x	Apollo4 Blue Plus Datasheet

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SECTION

1

Introduction

The Apollo4 Plus Family of SoCs is, at their core, low power devices. To maintain lowest power across the operating temperature range, Ambiq provides temperature-based voltage adjustments to the core and memory power rails to reduce power consumption. This application note describes how the voltage compensation over temperature is handled in software and how a user should implement this algorithm in their application.

List of Apollo4 Plus Family SoCs:

- AMAP42KP-KBR
- AMA4B2KP-KBR
- AMA4B2KP-KXR

SECTION

2

TEMPCO and VDDC_LV PRO Overview

The temperature compensation (TEMPCO) and power reduction optimizations take advantage of the on-chip temperature sensor coupled with a look-up table of voltage trim adjustments to operate at the lowest possible voltage. The ability of an Apollo4 Plus SoC to work properly with lower voltages at higher temperatures enables the device to maintain consistently low power from -20°C to +60°C by modifying certain internal voltages with respect to the on-chip measured temperature.

The following charts show the voltage after applying the temperature compensation algorithm over temperature.

The MRAM is located at the following position, as seen from the top side of the IC:

Figure 2-1: Voltage after Compression at 1.71V

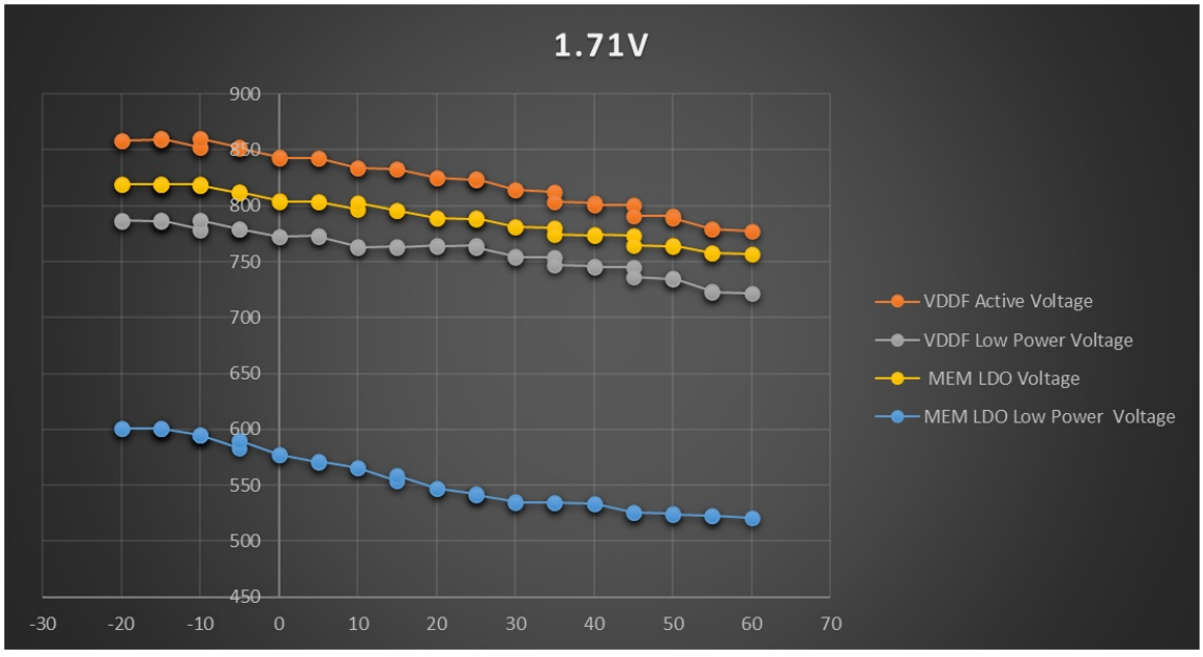


Figure 2-2: Voltage after Compression at 1.80V

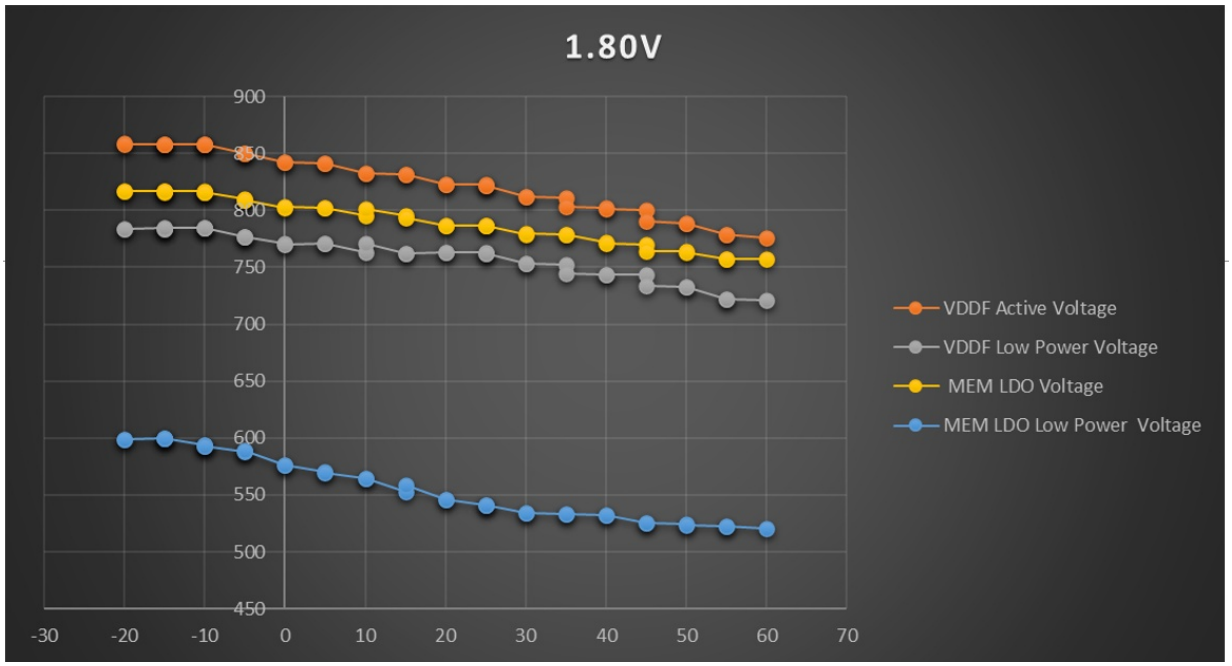
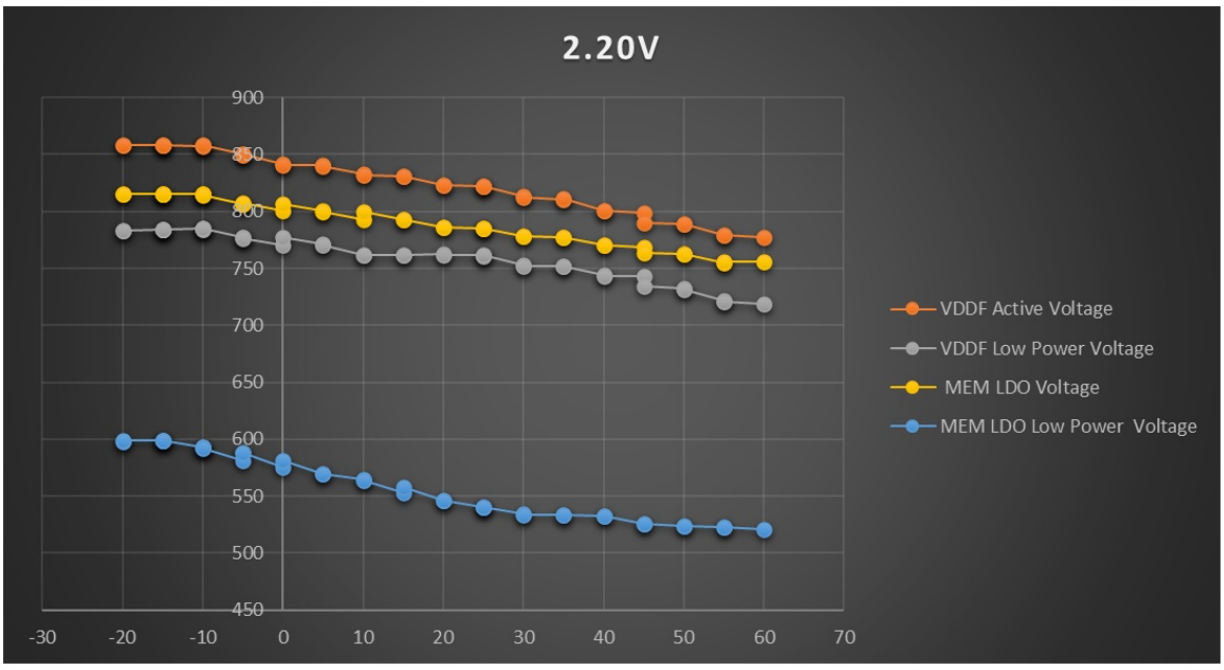


Figure 2-3: Voltage after Compression at 2.20V



The following table shows the expected current draw at 25°C (see footnote 2 in Table 2-1 on page 10) with and without temperature compensation and VDDC power optimization applied. This chart can also be found in the Apollo4 Plus family datasheets.

Table 2-1: Current Consumption in Active and Sleep Modes

Symbol	Parameter	Test Conditions	VDD (V)	Min	TYP (Without PRO)[1]	Typ (with PRO)[1]	Max	Unit
$I_{RUNLPFB}$[1,2,3,4,5]	Coremark run current	Executed from internal NVM, cache enabled, buck enabled, 128 kB TCM, HFRC=96 MHz	1.9	-	17.2	15.4	-	µA/ MHz
			3.3	-	9.9	8.9	-	
$I_{RUNHPFB}$[1,2,3,4,5]	Coremark run current	Executed from internal NVM, cache enabled, buck enabled, 128 kB TCM, HFRC=192 MHz	1.9	-	21.3	20.8	-	µA/ MHz
			3.3	-	12.3	11.9	-	
$I_{RUNWLPFB}$[1,2,3,4,5]	While loop run current	Executed from internal NVM, cache enabled, buck enabled, 8 kB TCM	1.9	-	8.6	7.2	-	µA/ MHz
			3.3	-	5.0	4.1	-	
I_{SS2}[1,2,3,4,5]	System Sleep mode 2 current	WFI instruction with SLEEP=1, clocks gated, oscillators on buck converters enabled, 8 kB TCM retained	1.9	-	180	180	-	µA
			3.3	-	103.6	103.6	-	
$I_{SDS2\text{-}8RET}$[1,3,4,5]	System Deep Sleep mode 2 current	WFI instruction with SLEEPDEEP=1, XTAL on, buck enabled, BLE off, 8 kB TCM retained	1.9	-	14.3	13.6	-	µA
			3.3	-	8.2	7.8	-	
$I_{SDS2\text{-}384RET}$[1,3,4,5]	Sleep Deep Sleep mode 2 current	WFI instruction with SLEEPDEEP=1, XTAL on, buck enabled, BLE off, 384 kB TCM retained	1.9	-	25.6	24.55	-	µA
			3.3	-	14.7	14.1	-	
$I_{SDS2\text{-}1900RET}$[1,3,4,5]	System Deep Sleep mode 2 current	WFI instruction with SLEEPDEEP=1, XTAL on, buck enabled, BLE off, 1.9 MB SRAM retained	1.9	-	61.75	58.1	-	µA
			3.3	-	35.6	33.5	-	
I_{SDS3}[1,3,4,5]	Sleep Deep Sleep mode 3 current	WFI instruction with SLEEPDEEP=1, XTAL off, buck enabled, BLE off, all SRAM off	1.9	-	13.4	13.4	-	µA
			3.3	-	7.72	7.72	-	

[1] Apollo Plus current consumption measurements are given with and without the optional software-enabled TEMPCO and VDDC_LV power reduction optimization (PRO).

[2] Core clock (HCLK) is 96 MHz for each parameter unless otherwise noted.

[3] All values are meaures at 25°C.

[4] Current consumption is normalized to 3.3V and shown for comparison purposes. Efficiency of conversion not considered. Specification at their VDD voltages available upon request.

[5] All I/O power domains and peripherals powered off.

To ensure the Apollo4 Plus SoC and system achieve the lowest power consumption over temperature, the application software needs to periodically call this temperature-based voltage adjustment routine. The algorithm needs be run every ten seconds or sooner to ensure low power consumption. The system designer should determine the appropriate frequency to not negatively impact user power, while not impacting overall system performance.

SECTION

3

TEMPCO and VDDC_LV PRO in the HAL

The Apollo4 Plus family HAL has been updated to include temperature compensation code in AmbiqSuite Release 4.3.0. The crypto section of the micro also uses these voltages. If you modify the VDDF and VDDF-LV voltages using the crypto boost code, you must rerun the TEMPCO algorithm immediately after to ensure proper voltage compensation.

The information below is an outline of how temperature compensation is performed in the TEMPCO example, in the power section of the SDK examples. Use **boards/apollo4p_evb/examples/power/tempco** as a reference. It is in the user's best interest to read the information and peruse the TEMPCO example to better understand the implementation. The following macro in **am_hal_pwrctrl.h** needs to be defined for this algorithm to take effect.

```
//*****************************************************************************
//
//! Option for the TEMPCO power minimum power.
//
//*****************************************************************************
#define AM_HAL_TEMPCO_LP
```

To implement TEMPCO, from a high-level, the application will:

1. Enable and initialize a timer with an appropriate TEMPCO period. Ambiq recommends a period of 10 seconds or sooner.
2. Call the **am_hal_pwrctrl_tempco_init()** function.
3. On each timer interrupt:
    a. Power up, enable, and initialize the ADC if not already.

```
am_hal_adc_power_control(g_ADCHandle, AM_HAL_SYSCTRL_WAKE, true);
am_hal_adc_enable(g_ADCHandle);
```

b. Obtain the required number of temperature samples from the ADC as defined by the macro **AM_HAL_TEMPCO_NUMSAMPLES** in the example.

```
adc_temperature_samples_get(AM_HAL_TEMPCO_NUMSAMPLES, g_sSamples);
```

c. Pass the samples to the TEMPCO handler, **am_hal_pwrctrl_tempco_sample_handler()**. This function makes necessary updates to the device voltages based on the temperature samples.

```
am_hal_pwrctrl_tempco_sample_handler(AM_HAL_TEMPCO_NUMSAMPLES,
g_sSamples)
```

d. To conserve power between samples if the ADC is not running constantly, the user may power down the ADC to conserve additional power.

```
am_hal_adc_power_control(g_ADCHandle, AM_HAL_SYSCTRL_DEEPSLEEP, true);
```

4. Restart timer from Step 1 above.
5. Repeat Steps 3 through 4.

SECTION

4

TEMPCO and VDDC_LV PRO Algorithm

The **TEMPCO** and **VDDC_LV PRO** Algorithm in the HAL consists of valid production trim data stored in the chip prior to shipping, an internal temperature relative to the time the algorithm is being run, and a lookup table provided by Ambiq.

The TEMPCO algorithm and initialization will perform the following sequence:

1. Check for valid trim data from production and proper number of samples.
2. Validate the temperature samples that were provided by the application.
3. If temperature samples are reliable:
    a. Average the samples and convert to the units for the lookup tables.
    b. Use lookup table to get trim settings with respect to temperature.
4. If the samples are not reliable, then for this cycle only, all voltage trims are reverted to factory settings to maintain the best system reliability.
5. Set the following trims per either #2 or #3.
    - VDDF active trim
    - VDDF LP trim
    - Mem LDO active trim
    - LDO LP trim

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