APPLICATION NOTE

Artasie AM18X5 System Power Management

Ultra-low power coupled with a highly sophisticated feature set

A-RTC185-ANGA01EN v2.0

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Revision History

Revision	Date	Description
1.0	February 2017	Initial Release.
1.1	June 2017	Added leakage management
1.2	July 2017	Corrected calculations in Section 9.1
1.3	August 2017	Updated doc to only reflect the AM18X5 part numbers
2.0	January 17, 2023	Updated document template

Reference Documents

Document ID	Description

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SECTION

1

Introduction

In addition to fundamentally low power real-time clock (RTC) operation, the Ambiq Artasie AM18X5 includes the capability to effectively manage the power of other devices in a system. This allows the creation of extremely power efficient systems with minimal additional components. This Application Note describes how the AM18X5 may be used in various applications.

SECTION

2

System Power Control Applications

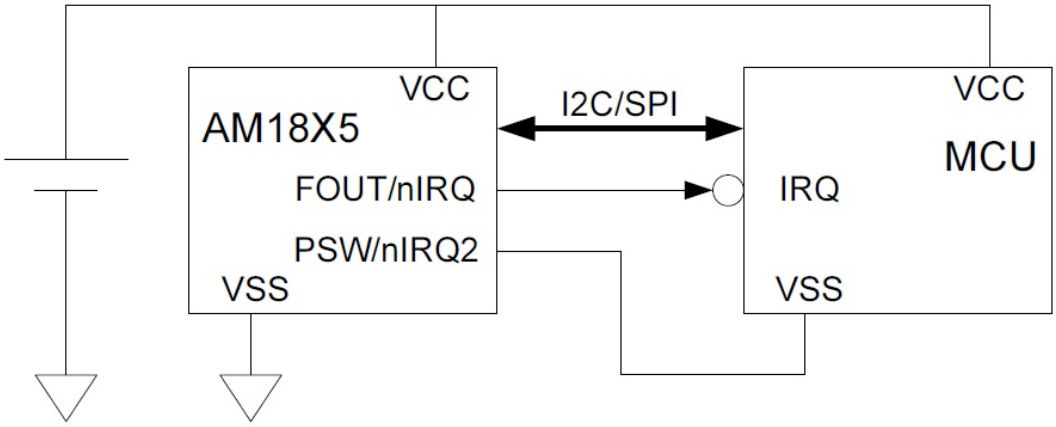
The AM18X5 enables a variety of system implementations in which the AM18X5 can control the power used by other elements in the system. This configuration is typically used when the entire system is powered from a battery and minimizing total power usage is critical.

2.1 VSS Power Switched

Figure 2-1 on page 9 shows the recommended implementation, in which the internal power switch of the AM18X5 is used to completely turn off the MCU and/or other system elements. In this case the PSW/nIRQ2 output is configured to generate the SLEEP function, and the PWR2 bit is asserted. Under normal circumstances, the PSW/nIRQ2 pin is pulled to VSS with ~1 ohm of resistance, so that the MCU receives full power. The MCU initiates a SLP operation, and when the AM18X5 enters the SLEEP state the PSW/nIRQ2 pin is opened and power is completely removed from the MCU. This results in significant additional power savings relative to the other alternatives because even very low power MCUs require more current in their lowest power state than the AM18X5.

The AM18X5 normally powers up selecting the OUTB register bit to drive the PSW/nIRQ2 pin, and the default value of the OUTB bit is zero. This ensures that the power switch is enabled at power up. If the power switch function is used, software should only change the PSW/nIRQ2 selection between OUTB (0b111) and SLEEP (0b110) to ensure no glitches occur in the power switching function.

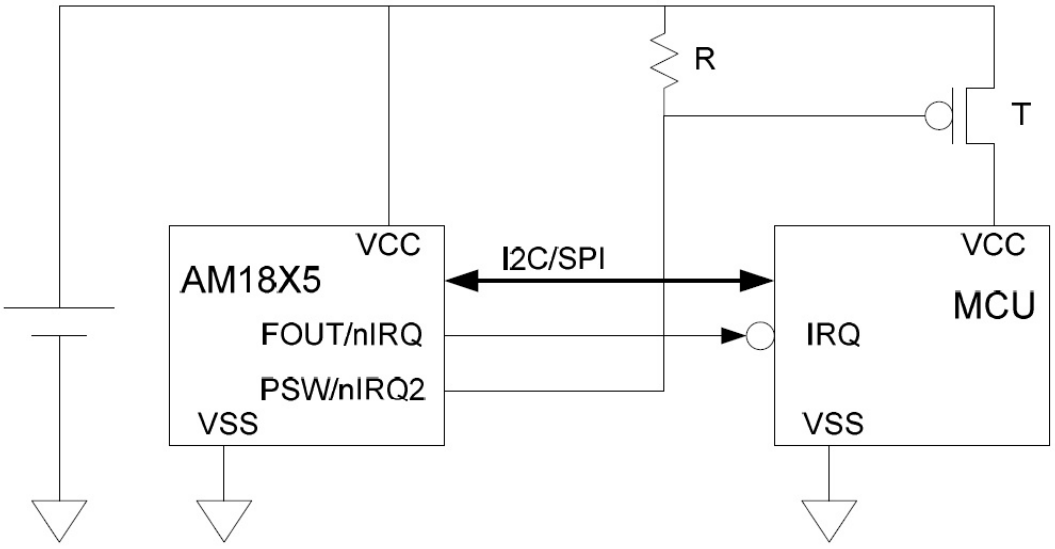
Figure 2-1: Switched VSS Power Control



2.2 VCC Power Switched

Figure 2-2 shows the application in which an external transistor switch T is used to turn off power to the MCU. The SLP function operates identically to the VSS switched case above, but this implementation allows switching higher current and maintains a common ground. R can be on the order of megohms, so that negligible current is drawn when the circuit is active and PSW/nIRQ2 is low.

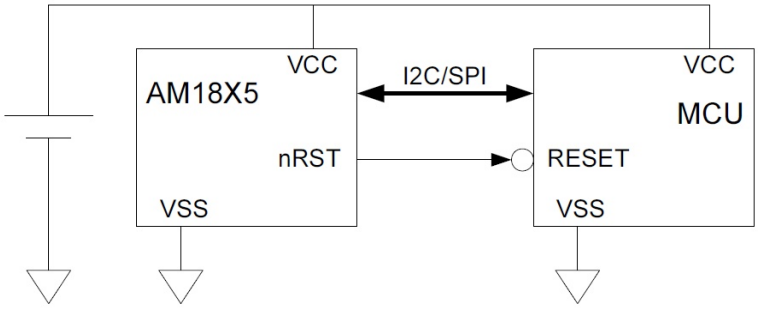
Figure 2-2: Switched VCC Power Control



2.3 Reset Driven

Figure 2-3 shows the application in which the AM18X5 communicates with the system MCU using the reset function. In this case the MCU initiates a SLP operation, and sets the SLRES bit so that when the AM18X5 enters the SLEEP state, it brings nRST low to reset the MCU. When the trigger occurs, the AM18X5 releases the MCU from reset, and may also generate an interrupt which the MCU can query to determine how reset was exited. Since many MCUs use much less power when reset, this implementation can save some system power.

Figure 2-3: Reset Driven Power Control

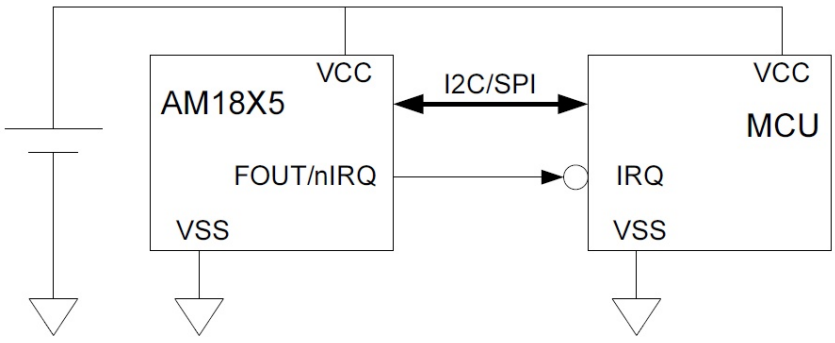


One potential issue with this approach is that many MCUs include internal pullup resistors on their reset inputs, and the current drawn through that resistor when the reset input is held low is generally much higher than the MCU would draw in its inactive state. Any pullup resistor should be disabled and the nRST output of the AM18X5 should be configured as a push-pull output.

2.4 Interrupt Driven

Figure 4 shows the simplest application, in which the AM18X5 communicates with the system MCU using an interrupt. The MCU can go into standby mode, reducing power somewhat, until the AM18X5 generates an interrupt based on an alarm or a timer function. This produces smaller power savings than other alternatives, but allows the MCU to wake in the shortest time.

Figure 2-4: Interrupt Driven Power Control



SECTION

3

Sleep Register

The register which controls the Sleep function of the Power Management system in the AM18X5 is the Sleep Register, accessed at register offset 0x17. The bits of the Sleep Register are defined below.

- **SLP [7]** - when 1, the Power Control State Machine (SM) described in Section 4will transition to the SWAIT state. This bit will be cleared when the SM returns to the RUN state. If either STOP is 1 or no interrupt is enabled, SLP will remain at 0 even after an attempt to set it to 1.
- **SLRES [6]** - when 1, assert nRST low when the Power Control SM is in the SLEEP state.
- **EX2P [5]** - when 1, the external interrupt XT2 will trigger on a rising edge of the WDI pin. When 0, the external interrupt XT2 will trigger on a falling edge of the WDI pin.
- **EX1P [4]** - when 1, the external interrupt XT1 will trigger on a rising edge of the EXTI pin. When 0, the external interrupt XT1 will trigger on a falling edge of the EXTI pin.
- **SLST [3]** - set when the AM18X5 enters Sleep Mode. This allows software to determine if a SLEEP has occurred since the last time this bit was read.
- **SLTO [2:0]** - the number of 7.8 ms periods after SLP is set until the Power Control SM goes into the SLEEP state. If SLTO is not 0, the actual delay is guaranteed to be between SLTO and (SLTO - 1) periods. If SLTO is 0, the transition will occur with no delay.

SECTION

4

Sleep Control State Machine

The AM18X5 includes a sophisticated Sleep Control system that allows the AM18X5 to manage power for other chips in a system. The Sleep Control system provides two outputs which may be used for system power control:

1. A reset (nRST) using the nRST output pin may be generated to put any host controller into a minimum power mode and to control sequencing during power up and power down operations.
2. A power switch signal may be generated (PWR), which allows the AM18X5 to completely power down other chips in a system by allowing the PSW/nIRQ2 pin to float. The OUT2S field must be set to a value of 6 to select the SLEEP output. When using the PWR output, PSW/nIRQ2 is configured as an open drain pin with 1 ohm resistance. This allows the AM18X5 to directly switch up to 50 mA of current with no external components or to control a single external transistor for higher current switching. The low resistance power switch is enabled by setting the PWR2 bit. If the I^2C or SPI master (i.e., the host controller) is powered down by the power switch, the PWGT bit should be set to ensure that a floating bus does not corrupt the AM18X5.
3. If OUT2S is 6, but the PWR2 bit is not set, PSW/nIRQ2 will be configured as a high true Sleep output which may be used as an interrupt.

The Sleep state machine in Figure 4-1 on page 14 receives several inputs which it uses to determine the current Sleep State:

1. **POR** – the indicator that power is valid, i.e. either VCC or VBAT is above the minimum voltage.
2. **SLP** - the Sleep Request signal which is generated by a software access to the Sleep Register.
3. **TRIG** - the OR of the enabled interrupt request from the Alarm comparison in the RTC, the interrupt signal from the Countdown Timer in the RTC, the interrupt signal from the Watchdog Timer in the RTC, the External Interrupt 1 or 2 pins, the Battery Low detection interrupt, the Autocalibration Fail interrupt, or the Oscillator Fail interrupt.

4. **TO** - the timeout signal from the SL Timeout counter.

4.1 RUN

RUN is the normal operating state of the AM18X5. PWR and nRST are not asserted, SLP is 0, and SLST holds the state of the previous Sleep. SLST should be cleared by software before entering the SWAIT state.

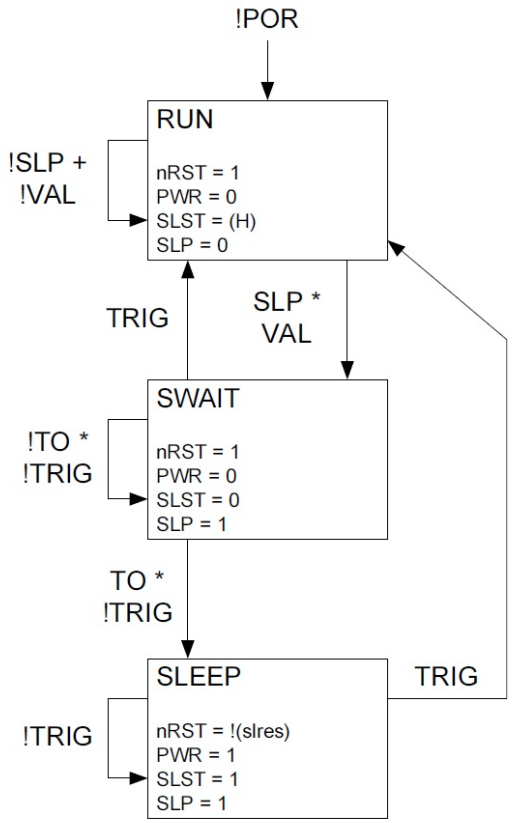
4.2 SWAIT

Software can put the chip to sleep by setting the SLP bit in the Sleep Register, as long as a valid interrupt is enabled (see *Section 4.4 SLP Protection on page 14*) indicated by VAL being asserted. The SM moves to the SWAIT state and waits for a programmable number of seconds (0 to 7) selected by the SLTO field in the Sleep Register. This allows software to perform additional cleanup functions after setting SLP before the MCU is shut down. Operation is the same in SWAIT as it is in RUN, and if an enabled interrupt occurs (TRIG) the SM returns to the RUN state and clears the SLP bit. PWR and nRST are not asserted, SLP is 1, and SLST is 0.

4.3 SLEEP

Once the programmed number of seconds has elapsed in the SWAIT state, the TO signal is asserted and the machine moves to the SLEEP state, putting the AM18X5 into Sleep Mode. In this case the PWR signal is removed, and nRST is asserted if SLRES is set. Once an enabled operational interrupt occurs (TRIG), the SM returns to the RUN state, reactivates power and removes reset as appropriate. The SLST register bit in the Sleep Register is set when the SLEEP state is entered, allowing software to determine if a SLEEP has occurred.

Figure 4-1: Sleep State Machine



4.4 SLP Protection

Since going into Sleep Mode may prevent an MCU from accessing the AM18X5, it is critical to ensure that the AM18X5 will receive a TRIG signal. To guarantee this, the SLP signal cannot be set unless the STOP bit is 0 and at least one of the following conditions exists:

1. The AIE bit is 1, enabling an Alarm interrupt.
2. The TIE and the TE bits are 1, enabling a Countdown Timer interrupt.
3. Either the EX1E or EX2E bit is a 1, enabling an External interrupt.
4. The BMB field is not zero and the WDS bit is zero, enabling a Watchdog Interrupt

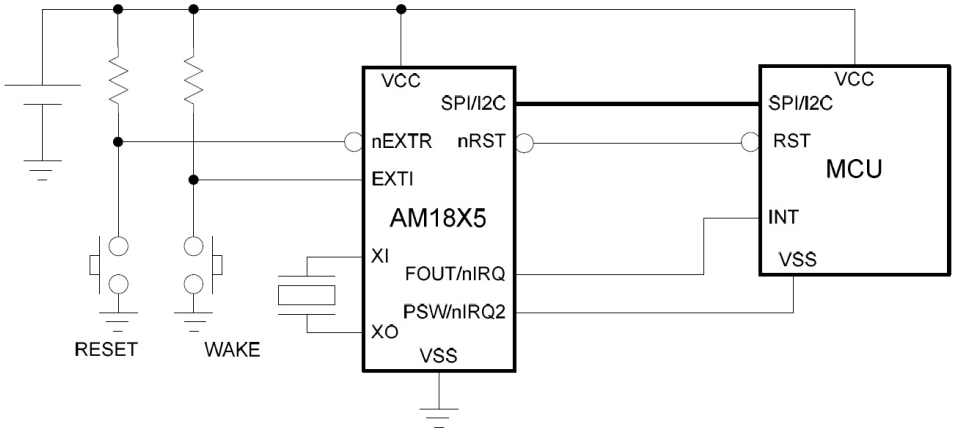
In addition, SLP cannot be set if there is an interrupt pending. Software should read the SLP bit after attempting to set it. If SLP is not asserted, the attempt to set SLP was unsuccessful either because a correct trigger was not enabled or because an interrupt was already pending. Software must correct the situation before attempting to enter Sleep Mode again.

SECTION

5 Typical System Implementation

Figure 5-1 is a more detailed view of a typical system using the VSS Power Switched approach. The VSS pin of the MCU, and potentially other system components, is switched using the PSW pin of the AM18X5. The nIRQ pin of the AM18X5 is connected to an interrupt input of the MCU, allowing the MCU to utilize the RTC interrupt functions of the AM18X5 when it is awake. The nRST output of the AM18X5 is connected to the reset input of the MCU, enabling the AM18X5 to control power on reset and integrate an external MCU reset button RESET. The MCU controls the AM18X5 over a SPI or I^2C I/O channel.

Figure 5-1: System Example



The key value of the AM18X5 in this type of system is the ability to put the MCU into an off state, and providing a very rich variety of triggers which can cause the AM18X5 to wake the MCU from the off state. There are a number of different triggers which may be useful.

5.1 Alarms

The system may require the MCU to wake up at particular times, which is accomplished by configuring the Alarm Interrupt function of the AM18X5.

5.2 Countdown Timer

The system may require the MCU to wake up at periodic intervals which do not necessarily correspond to specific calendar times. The Countdown Timer of the AM18X5 provides highly flexible time interval configuration to support this function.

5.3 WAKE Button/Switch

A very common requirement is the capability to wake the system with a manual input such as a pushbutton or switch, typified by the WAKE button in Figure 5-1 on page 15. One of the external interrupt inputs such as EXTI may be simply connected to the button. All AM18X5 inputs include Schmitt trigger circuitry to enable clean interrupts. If additional debouncing of the input is required, the AM18X5 provides direct access to the interrupt input pins to facilitate software implementations.

5.4 External Device Inputs

In some systems an external device such as a wakeup radio may provide a signal which must wake the MCU. An AM18X5 external interrupt such as the WDI pin provides this capability.

5.5 Analog Inputs

Some systems include analog signals, such as light sensors or detectors on radio antennas, which must wake the MCU. The Analog Comparator function, which allows the voltage on the VBAT input of the AM18X5 to be compared with a configurable voltage threshold and generate an interrupt, can easily be used in this application, and it allows flexible configuration, both in voltage levels and in transition direction to support different environments. The Analog Comparator may also be used to provide a third external digital interrupt if necessary by selecting the proper digital threshold.

5.6 Battery Low Detection

The Analog Comparator can provide a battery low detection function. In this case, the VCC pin would be tied to the VBAT pin, and the thresholds would be adjusted to ensure that the Battery Low interrupt occurs prior to any Brownout Detection on the VCC input. This allows software to prepare for a potential battery failure in advance without having to poll the battery level.

5.7 Errors

Any failure interrupt in the AM18X5 may also be configured to wake the MCU. This can be particularly valuable for Oscillator Failure detection, when software may need to respond to the error in order to report the problem quickly.

SECTION

6

Saving Parameters

If the MCU is powered down in Sleep Mode, there is often some data which must be preserved until the next power up. The internal RAM of the AM18X5 is always available, so software can easily save any necessary parameters prior to entering Sleep Mode and retrieve them when the MCU wakes up.

SECTION

7

Power Switch Electrical Characteristics

The power switch on the AM18X5 PSW pin has a typical on resistance of 1 ohm over the full temperature range so that currents up to 50 mA may be handled without appreciable voltage drop. This allows the AM18X5 to switch power to multiple devices in most systems, which can be particularly important for components without internal Sleep functions. If the PSW pin is not used as a power switch, the maximum leakage current of the ~1 Ω switch is less than 250 pA at 25°C.

SECTION

8

Avoiding Unexpected Leakage Paths

One potential problem which can occur when the AM18X5 powers other devices down is that unexpected leakage paths can be created between the powered AM18X5 and the unpowered device. The AM18X5 can be configured to disable inputs and outputs in Sleep Mode to prevent leakage. In general, any input or output pin connected to a device which is powered down should be disabled. Any pins which remain powered in Sleep Mode, such as pushbutton inputs used to wake the system, must not be disabled.

1. nRST is disabled in Sleep Mode by clearing the RSEN bit in the Output Control Register.
2. FOUT/nIRQ is disabled in Sleep Mode by clearing the O1EN bit in the Output Control Register.
3. CLKOUT/nIRQ3 is disabled in Sleep Mode by clearing the O4EN bit in the Output Control Register.
4. nTIRQ (I^2C devices only) is disabled in Sleep Mode by clearing the O3EN bit in the Output Control Register.
5. EXTI is disabled in Sleep Mode by setting the EXDS bit in the Output Control Register.
6. WDI is disabled in Sleep Mode by setting the WDDS bit in the Output Control Register.
7. The I^2C or SPI interface pins are disabled in Sleep Mode by setting the PWGT bit in the Oscillator Control Register. This is a particularly important function because there are multiple leakage paths in the I/O interfaces.

SECTION

9

System Power Analysis

The AM18X5 can significantly improve the power characteristics of many different types of systems. A specific example will be presented, and several other generalizations can be made from this. The fundamental advantage provided by the AM18X5 is that it allows the system designer to essentially ignore the sleep current of other system components, which allows the utilization of components which have be optimized for other parameters, such as active power, cost or functionality.

9.1 Using an External RTC with Power Management

The key element in any system power analysis is the usage profile, and for this example we assume the system is active for T_{act} and inactive for T_{inact}. I_{act} is the current drawn when the system is active, and I_{inact} is the current drawn when the system is inactive. The average current I_{avg} is therefore:

$$I_{avg} = (T_{act} * I_{act} + T_{inact} * I_{inact})/(T_{act} + T_{inact})$$

An example will use a PIC16LF1947 MCU, which is highly optimized for low power operation. This MCU draws 80 nA in Sleep Mode, 1.8 uA in Sleep Mode with the internal oscillator and RTC active, and 120 uA in 500 KHz active mode. Assume a usage profile where the system in active for 1 second every 30 minutes, so that Tact is 1 and Tinact is 1799. If this MCU is used alone and supplies the RTC functions, the average current for the usage profile is:

$$I_{avg} = (1 * 120\ \mu A + 1799 * 1.8\ \mu A)/1800 = 1.865\ \mu A$$

If the AM18X5 is used to provide the RTC functionality in Autocalibrated RC Mode (<20 nA continuous current) and the PIC is placed into Sleep Mode, the average current for the usage profile is dramatically lower:

$$I_{avg} = (1 * 120\ \mu A + 1799 * 80\ nA)/1800 + 20\ nA = 166\ nA$$

This is a significant improvement, but the current can be further reduced by having the AM18X5 switch power to the MCU. The resulting average current is ~50% lower:

I_{avg} = (1 * 120 µA + 1799* 0 nA)/1800 + 20 nA = 86 nA

9.2 Managing MCU Active Power

In many cases, the duration of the active time is a function of how much processing must be accomplished, and can therefore be assumed to be a linear function of the MCU clock frequency in active mode. The examples in the previous section assumed that the MCU ran for 1 second at 500 KHz, so 500,000 cycles of an 8-bit processor were required. Like most MCUs, the PIC has a relatively constant active current as a function of clock frequency, so using a higher internal frequency in the same MCU would have little effect on the overall power. However, there may be other MCUs (such as those with 32-bit processors) which have better active power efficiency but poor sleep power, and power switching with the AM18X5 eliminates any sleep power considerations.

9.3 Lower Cost MCUs

Lower cost MCUs often have poor sleep power characteristics relative to sleep optimized parts. Since the AM18X5 eliminates sleep power considerations, these lower cost processors may provide equivalent overall average power at significant cost savings.

9.4 High Performance Processors

In some applications very high performance processors such as DSPs must be used due to real time processing requirements. These processors are generally not optimized for sleep performance, but they may be used in applications with low duty cycles. One example of this is fingerprint recognition, which is rarely accessed but must provide very fast response with complex processing. The AM18X5 power management functions enable a system design where the processor is powered down the vast majority of the time, providing low average power combined with very high instantaneous performance.

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A-RTC185-ANGA01EN v2.0
January 2023