APPLICATION NOTE

Artasie AMX8X5 Counter Loss

Ultra-low power coupled with a highly sophisticated feature set

A-RTCX85-ANGA03EN v2.0

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Revision History

Revision	Date	Description
1.0	February 2017	Initial Release.
2.0	January 18, 2023	Updated document template

Reference Documents

Document ID	Description

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SECTION

1 Introduction

Under certain rare circumstances, the combination of low I^2C clock frequencies and very frequent burst read references to the AMX8XX Calendar counters can cause a small time loss from the Calendar counters. This document describes experiments which quantify the possible loss.

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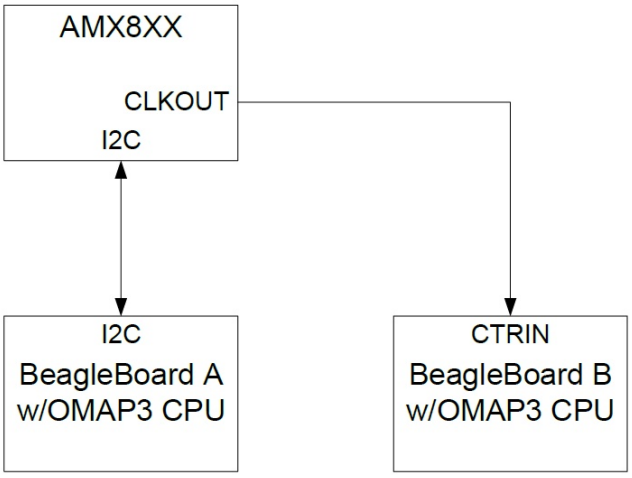
Measurement Methodology

Because the time losses are very small, measuring them accurately is challenging. Ambiq has created a measurement system to specifically address the issue of measuring these small changes over long time periods, which is typically not feasible with commercial frequency counters. The system is shown in Figure 2-1.

Figure 2-1: Measurement System



The BeagleBoard is a commercially available processing system built around a Texas Instruments OMAP3 high performance processor. Two BeagleBoards are used in the measurement system, and each has been modified to use a 26 MHz TCXO to provide the fundamental input clock for high accuracy. BeagleBoard A is used to control the AMX8XX via the I^2C interface (the SPI interface may also be used). The AMX8XX is configured to drive a clock onto the CLKOUT pin, typically the 1 second clock which drives the Calendar counters. The CLKOUT pin is connected to a counter/timer input CTRIN of BeagleBoard B, and software on this BeagleBoard allows the length of each clock period to be captured with a precision of ± 40 ns and stored in local memory. This data is then extracted and extensive data analysis is performed. Up to 250,000 clock cycles may be captured (almost 3 days if seconds are captured), allowing very precise measurements over very long time periods.

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3

Loss vs I²C Frequency Results

A set of experiments modified the I²C frequency while performing burst reads of the Counter Registers (offsets 0 to 7) with no gaps between bursts. Table 3-1 contains the results of a series of runs with I²C frequencies from 10000 Hz to 100000 Hz (10 kHz to100 kHz). Each column will be explained below. Note that all of these runs were performed with typical silicon at 25°C.

Table 3-1: I²C Frequency Variation Data

I²C Freq (Hz)	Ref Per Sec	Bursts	Total Time (s)	Error (ppm)	Error @ 100 Refs/second (ppm)	Error Cycles	EC Per Million	Time Error (ms)	Time Error per Cycle (ms)
10000	95.45	2100000	22000.65	28.61	29.97	44	20.95	629.455	14.306
11000	105.16	2200000	20920.9	35.39	33.65	71	32.27	740.341	10.427
12000	114.55	2000000	17460	26.99	23.56	36	18.00	471.255	13.090
15000	142.78	2000000	14007.8	23.89	16.74	34	17.00	334.703	9.844
20000	189.87	3000000	15800.1	23.83	12.55	39	13.00	376.445	9.652
25000	236.60	4000000	16906	27.81	11.75	47	11.75	470.088	10.002
30000	284.94	4000000	14038	24.92	8.75	35	8.75	349.807	9.994
35000	331.10	4000000	12081	15.89	4.80	19	4.75	191.988	10.105
40000	376.44	4000000	10626	21.50	5.71	23	5.75	228.429	9.932
45000	420.92	6000000	14254.5	18.19	4.32	26	4.33	259.261	9.972
50000	468.11	6000000	12817.5	23.13	4.94	30	5.00	296.283	9.876
75000	689.27	13775000	19985	15.20	2.21	31	2.25	303.856	9.802
100000	941.97	12000000	12739.2	0.00	0.00	0	0.00	0.000	0

3.1 I^2C Freq

This is the frequency of the I^2C bus in Hz.

3.2 Refs Per Sec

This is the number of burst reads per second which are performed when 8-byte bursts are executed with no delay between them. This is the maximum possible burst frequency for each I^2C clock frequency.

3.3 Bursts

This is the total number of read bursts executed in the run.

3.4 Total Time

This is the time in seconds which the entire run took. This time is between 3 and 6 hours for each experiment.

3.5 Error

This is the deviation in parts per million (ppm) of the time measured in the Counters as compared to the correct time as measured by the precise BeagleBoard clock.

3.6 Error @ 100 Refs/Second

Under the assumption that an error has equal probability on each burst read, this is the time difference in ppm normalized to 100 burst reads per second.

3.7 Error Cycles

For each run, the pattern of one second period lengths shows that only a few cycles contain errors. This column contains the number of such cycles in each run.

3.8 EC Per Million

This is the number of error cycles per million overall cycles, which normalizes the error cycle numbers.

3.9 Time Error

This is the overall time deviation which occurred during the run in milliseconds.

3.10 Time Error Per Cycle

This is the time deviation created by each error cycle in milliseconds. Note that this error is always very close to 10 ms, which shows that the problem is caused by a synchronization between the I^2C clock and the 100 Hz clock which drives the Calendar counter chain. This also indicates that the maximum time deviation for any single burst reference will be no more than 10 ms at bus frequencies above 12 kHz.

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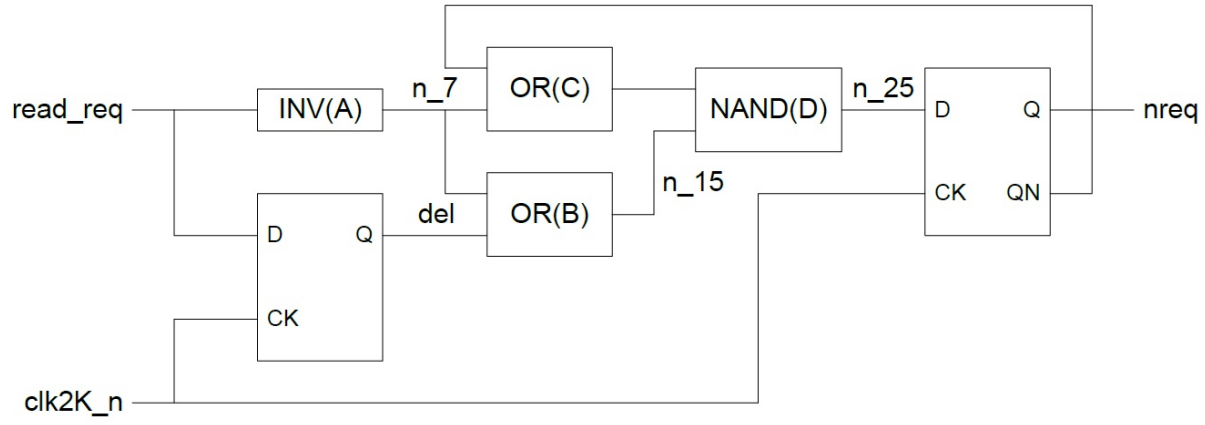
Error Mechanism Details

The physical experiments described above identified clock synchronization as the likely cause of the time loss. At that point, chip simulations were run to isolate the exact problem. The clock loss occurs due to a synchronization error between a burst read request clocked by the I^2C/SPI clock and the 2 kHz clock from the counter timing chain. The 2 kHz clock is divided by 20.48 to create the 100 Hz timing clock, and the 2 kHz clock also clocks a number of flip flops which are used to hold off the 100 Hz clock when a read to the Calendar Counters is occurring, in order to insure that the values read from all of the Counters is consistent (e.g., no counter rolls over during the read).

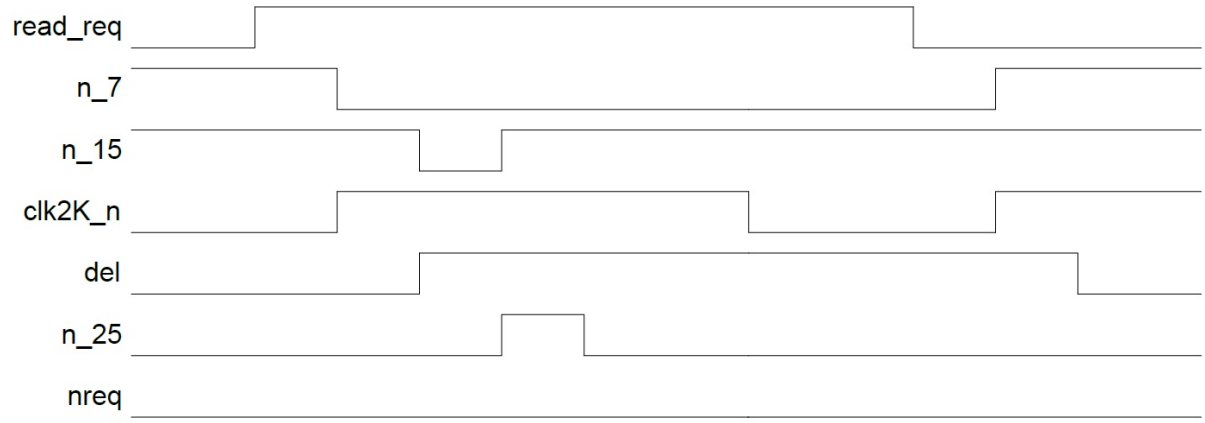
The circuit in Figure 4-1 is used to generate a version of the read request synchronized to the negative edge of the 2 kHz clock clk2K (the rising edge of clk2K_n). When read_req is asserted, under normal circumstances the output nreq is set on the next edge of clk2K_n, and the delayed version of the request del is asserted on that edge so that nreq is asserted for one cycle.

Figure 4-1: Synchronization Circuit



However, this circuit contains a race as shown in the timing diagram of Figure 4-2. If the edge of clk2K_n occurs just after the edge of read_req, the del flop will capture the read_req, but the delays in gates A, B, C and D will cause n_25 to be asserted too late and the nreq flop will not be asserted. The del flop will then remove n_15 and n_25 so that nreq never goes high. This condition is referred to as a “sync error”.

Figure 4-2: Synchronization Race Error



The window in which this error can occur is essentially the delays through the gates A, B, C and D (in the actual design C and D are part of the same OAI gate). For the worst case (at -40 °C) this delay is on the order of 1520 ns. Since the period of clk2K_n is 488 us, any particular reference can produce an error (a lost nreq) with a probability of (1520/488281) = 0.0031 = 0.31 %. This probability (probsync) drops significantly as the temperature increases, as shown in Table 4-1(all values are for worst case slow silicon). This occurs because the delay drops significantly at slightly higher temperatures.

Table 4-1: Sync Error Probability

Temperature	probsync
-40°C	0.31%
-25°C	0.07%
25°C	0.025%

A sync error can cause the actual loss of a 100 Hz clock only if it occurs during the cycle in which the 100 Hz generation logic would produce a clock cycle (the 100 Hz clock is typically asserted for one period of clk2K). Because nreq is not asserted, logic which normally delays the clock pulse until the read is complete is not active, so the clock is gated by the read and lost. The probability of a clock loss due to a sync error is a function of the length of the AMX8XX internal read request. The length of the read request is a function of the I^2C clock period and the number of Counters which are read in the burst, defined by:

length = I^2C clock period x (# of bytes read x 9)

The probability that a sync error will cause the loss of a 100 Hz clock (prob100) is roughly:

prob100 = 0.1 * (length in ms – 0.850)

If length is less than 0.85 ms, no errors can occur (prob100 = 0). For each burst length, this defines a minimum I^2C clock frequency above which correct operation is guaranteed, as shown in Table 4-2.

Table 4-2: Maximum Bus Frequency

Length (B)	I^2C Period (µs)	I^2C Frequency (kHz)
1	94.444	10.59
2	47.222	21.18
3	31.481	31.76
4	23.611	42.35
5	18.889	52.94
6	15.741	63.53
7	13.492	74.12
8	11.806	84.71

In order to verify the minimum frequency assertion, an AMX8XX slow corner silicon part was run at 83.33 kHz at -40 °C for 12 hours at the maximum 8-byte burst rate, which included 30,000,000 burst reads. No errors occurred during this test.

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Conclusions

For a single burst read, the probability that a 100 Hz clock cycle will be lost (problost) is given by:

problost = probsync * prob100

Table 5-1 shows the error rate and the absolute error in milliseconds/day for several I^2C clock frequencies and burst frequencies, assuming that the specified burst frequency occurs continuously and the system is at -40 °C. Note that for burst rates below 1 per second, the error is expressed in parts per billion (ppb).

Table 5-1: Error Summary

I^2C Freq (Hz)	Error Rate at Burst Frequency				Milliseconds/Day at Burst Frequency			
	10/sec (ppm)	1/sec (ppm)	1/min (ppb)	1/15 min (ppb)	10/sec	1/sec	1/min	1/15 min
10000	197.68	19.77	329.46	21.96	2287.79	228.79	3.813	0.254
20000	85.61	8.56	142.68	9.51	990.83	99.08	1.651	0.110
30000	48.25	4.83	80.42	5.36	558.47	55.85	0.931	0.062
40000	29.57	2.96	49.29	3.29	342.29	34.23	0.570	0.038
50000	18.37	1.84	30.61	2.04	212.58	21.26	0.354	0.024
60000	10.90	1.09	18.16	1.21	126.11	12.61	0.210	0.014
75000	5.56	0.56	9.26	0.62	64.34	6.43	0.107	0.007
85000	0	0	0	0	0	0	0	0

Based on the equations, for any particular I^2C frequency a maximum burst frequency can be determined which is guaranteed to produce no more than a specified error. Since the AMX8XX XT Oscillator can only be calibrated to 2 ppm, an error of 2 ppm can reasonably be assumed to be negligible. Table 5-2 on page 16 below shows the maximum burst frequency for various error values and I^2C frequencies. For example, if the I^2C clock is 50 kHz, a burst rate less than 1.09 bursts/second will produce a maximum error less than 2 ppm.

Table 5-2: Maximum Burst Rates

I^2C Freq (Hz)	Maximum Bursts/Second		
Max ppm ->	**1**	**2**	**5**
10000	0.05	0.10	0.25
20000	0.12	0.23	0.58
30000	0.21	0.41	1.04
40000	0.34	0.68	1.69
50000	0.54	1.09	2.72
60000	0.92	1.84	4.59
70000	1.80	3.60	8.99
85000	N/A	N/A	N/A

It is important to note that the above time losses are for continuous burst reads at the specified rate. Continuous high burst rates will require significant current to be drawn in the system, as shown in Table 5-3 for 8-byte burst reads from the Counters. The currents shown are only the average current in the I^2C pullup resistors, which are assumed to be 10 kΩ with VCC at 3 V. Both the MCU and the AMX8XX will draw additional current during any I^2C transaction which will be in addition to the current shown in the table. This shows that if frequent burst reads are required, the I^2C frequency must be much higher than 10 kHz in order to minimize power dissipation which will therefore produce insignificant time loss.

Table 5-3: Burst Read Power Requirements

I^2C Freq	Xfer Length (ms)	Current at Burst Frequency (nA)			
		10/sec	**1/sec**	**1/min**	**1/15 min**
10000	10.4765	31430	3143	52	3
20000	5.2667	15800	1580	26	2
30000	3.5095	10529	1053	18	1
40000	2.6565	7970	797	13	1
50000	2.13625	6409	641	11	1
75000	1.4508	4352	435	7	0
100000	1.0616	3185	318	5	0

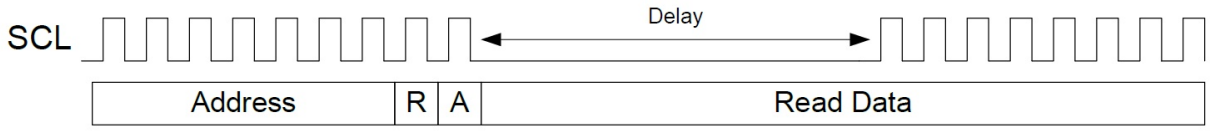
SECTION

6

Delay Between Read Address and Data

A question has been asked about the case where a delay is inserted between the I^2C read address transaction and the burst read data, as shown in Figure 6-1. If this sequence occurs, the Delay value is added to the transfer length shown in Table 5-3 on page 16 and changes the effective I^2C clock frequency. For example, an I^2C clock frequency of 50 kHz with a 3 ms delay inserted in every burst read is equivalent to a 20 kHz clock frequency. This would increase both the error frequency from Table 5-1 on page 15 and the average power from Table 5-3 on page 16. However, this stretching of SCL can only be caused by either the I^2C Master (the MCU) or the accessed slave (the AMX8XX). There is no reason that a Master would ever stretch SCL in this way, since it would slow down the bus and result in increased power dissipation. The AMX8XX never stretches SCL, so this sequence should never occur.

Figure 6-1: Read Transactions Delay



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