APPLICATION NOTE

Artasie AMX8X5 Startup Timing

Ultra-low power coupled with a highly sophisticated feature set

A-RTCX85-ANGA06EN v2.0

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Revision History

Revision	Date	Description
1.0	February 2017	Initial Release
1.1	June 2017	Changed the TIM flag usage description in section 3
2.0	January 19, 2023	Updated document template

Reference Documents

Document ID	Description

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SECTION

1

Introduction

This document describes the voltage and temperature dependent AMX8XX startup timing behavior of the 32.768 kHz crystal oscillator and the FOUT pin when power is applied to the VCC pin (after the AMX8XX has been in the reset state). If a 32.768 kHz crystal is attached the AMX8XX XI/XO pins, it will begin oscillating after the AMX8XX power on process completes because the AMX8XX starts up in XT mode by default. The FOUT pin also changes state during the AMX8XX power on sequence and is used to indicate to the host controller when the AMX-8XX is accessible via the I^2C or SPI serial interface. This is described in more detail in *Section 3.9 Power On AC Electrical Characteristics* and *Section 4.12.4 Power Up Timing in the AM08XX and AM18XX Datasheets*, version 0.90.

SECTION

2

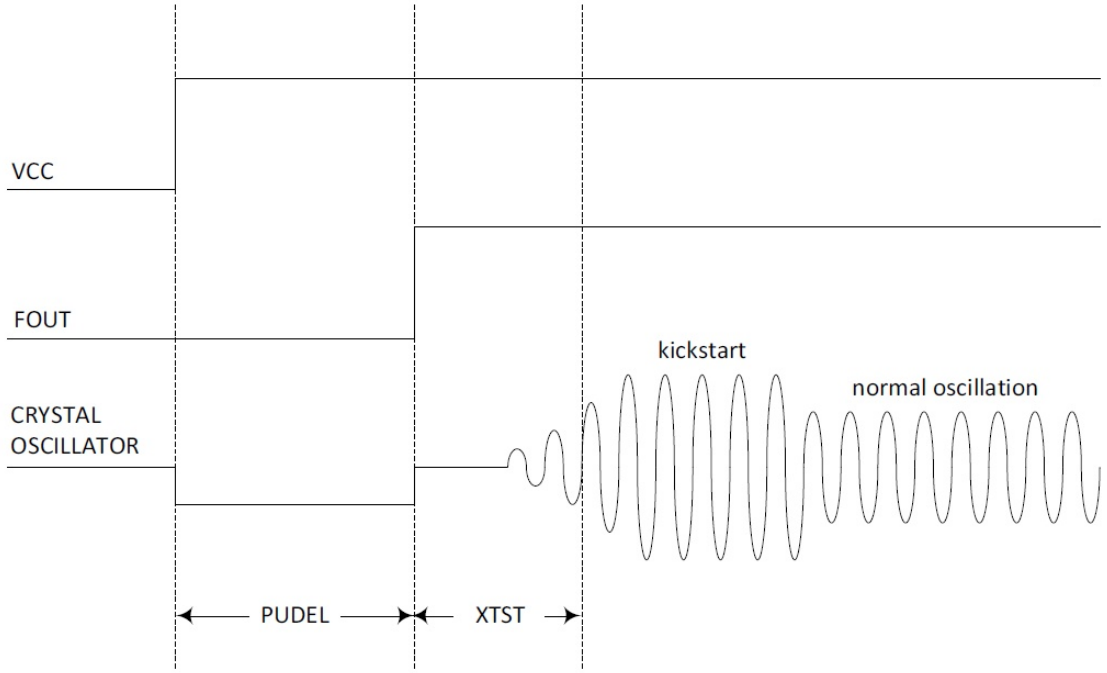
FOUT and Crystal Oscillator Startup Timing

When the voltage levels on the VCC and VBAT pins are below their minimum operating voltages, the AMX8XX enters the reset state. While in the reset state, the FOUT pin will be output low and the 32.768 kHz crystal oscillator (bias current) will be turned off. The AMX8XX will begin the power up process when the VCC voltage rises above the minimum VCC startup voltage (please see the V_{CCST} parameter in the AM08XX and AM18XX datasheets). The FOUT pin will remain low and the AMX8XX will remain in the reset state until the power up process completes and the ultra-low power internal voltage and current references have stabilized. After the power up process completes, the AMX8XX will exit the reset state and the following will occur.

1. The FOUT pin will go high (requires a pull-up resistor) which will enable I^2C or SPI interface access to the AMX8XX. The host controller should use the logic high output on FOUT to determine when the AMX8XX is accessible via the I^2C or SPI interface.
2. A bias current will be applied to the 32.768 kHz crystal oscillator circuit, which will cause it to begin oscillation. There is also an initial kick start applied to the crystal oscillator circuit to improve startup time and provide a more robust and reliable startup.

A timing diagram of the FOUT and crystal oscillator startup behavior is in Figure 2-1 on page 8. The PUDEL parameter is the AMX8XX power up delay from the time VCC is applied until FOUT goes high. The XTST parameter is the time required for the crystal oscillator amplitude to reach 200mV after FOUT goes high.

Figure 2-1: Timing Diagram of the FOUT and Crystal Oscillator Startup Behavior



Due to the ultra-low power architecture of the AMX8XX, the power up process and startup time required will increase at lower voltages and temperatures. Figure 2-1 and 2 below show the typical FOUT and crystal oscillator startup timing vs. voltage at temperatures below 25°C.

Figure 2-2: FOUT Startup Delay

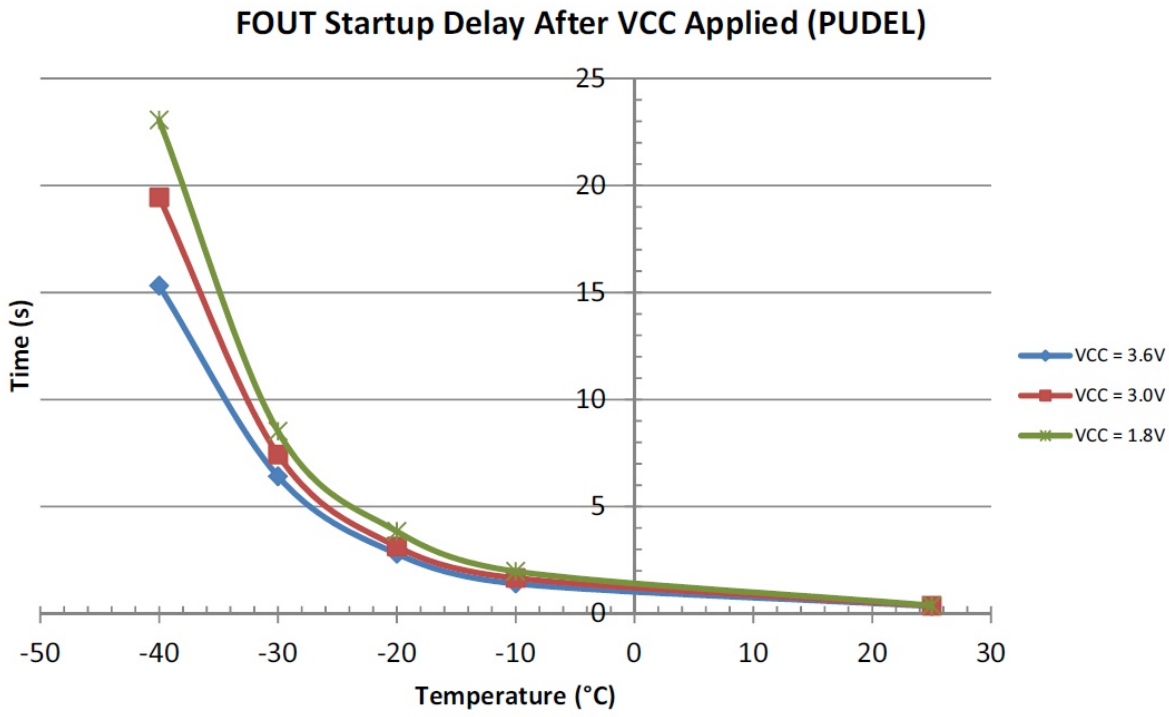
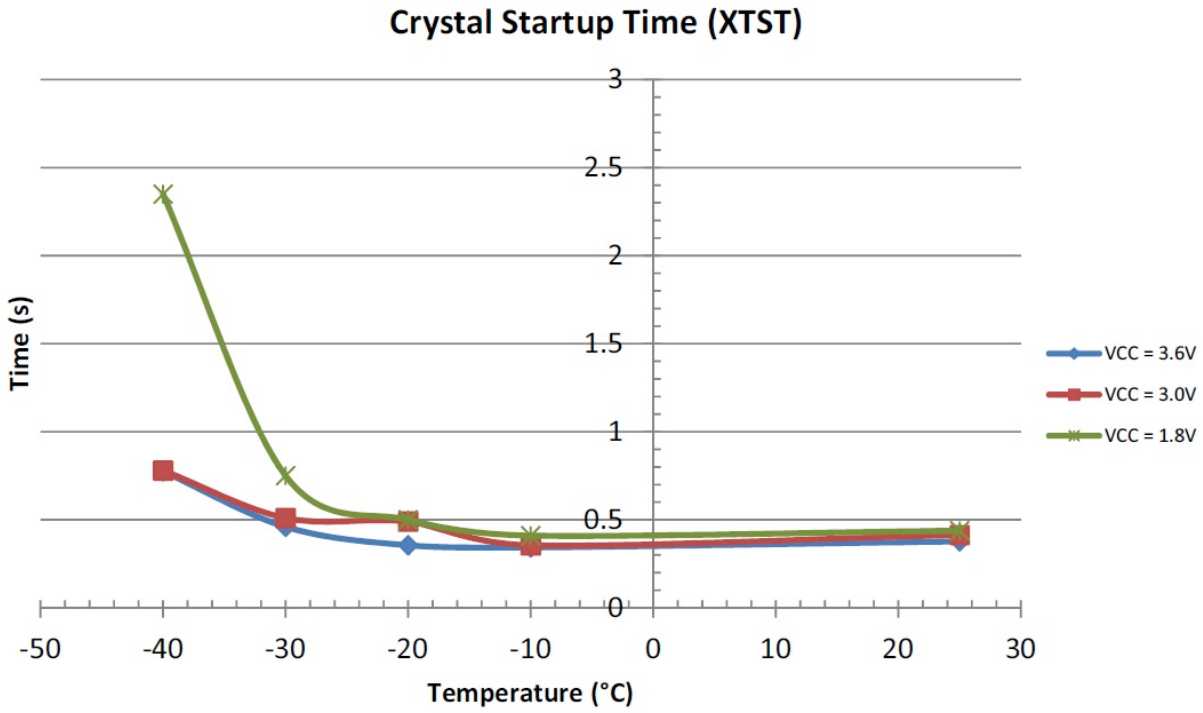


Figure 2-3: Crystal Startup Time



SECTION

3

Layout Guidelines

In the customer's application, the state of the FOUT pin must be monitored by the host controller to determine when access to the AMX8XX RTC becomes available. This ensures I^2C or SPI bus transfers do not happen too early, which will cause read/write failures. After the AMX8XX completes the power up process and bus access is available, the 32.768 kHz crystal will begin oscillating. At VCC = 3.0V, the crystal oscillator typically starts up and reaches sufficient amplitude in less than 1 second after FOUT goes high, so the host controller can simply wait the time shown in Figure 2-3 on page 9 above to ensure the crystal has started and has reach sufficient amplitude.

Alternatively, the countdown timer can be used to count the number of 32.728 kHz clock cycles that have occurred. After FOUT goes high, the countdown timer can be programmed to trigger a TIRQ interrupt when the crystal oscillator has been running for approximately 1 second (~32768 crystal clocks have occurred and the TIM flag gets set), which ensures the crystal oscillator has reached sufficient amplitude and the internal 32.768 kHz clock is stable. For example, the countdown timer frequency can be set to 64 Hz and the countdown timer register value set to 63, which will generate a countdown timer period of about 1 second. To check when the countdown timer reaches zero, the host controller can either poll the TIM flag bit, or wait for the TIRQ interrupt to occur.

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