DATASHEET

Apollo510 Lite SoC
Apollo510B Lite SoC
Apollo510D Lite SoC

Ultra-low Power Apollo510 Lite Series SoCs

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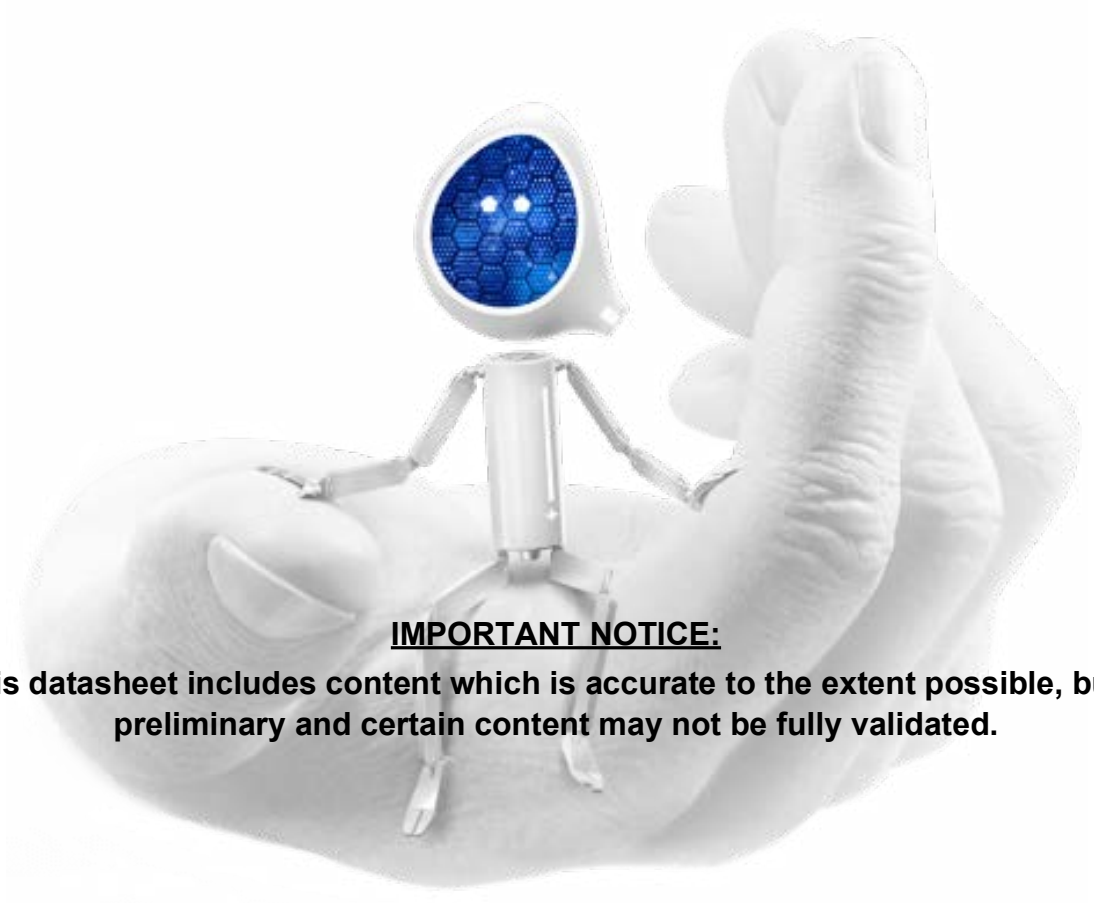


IMPORTANT NOTICE:

This datasheet includes content which is accurate to the extent possible, but is preliminary and certain content may not be fully validated.

Features

Arm® Cortex®-M55 Processor with Helium™ Technology

- 96 MHz / 192 MHz / 250 MHz operating modes
- Helium (MVE) vector integer, floating point
- Scalar half, single, and double-precision floating-point
- Supports Arm® TrustZone® security extensions
- Integrated 32 kB Instruction Cache and 32 kB Data Cache
- Integrated 256 kB Instr./Data Tightly Coupled Memory (TCM)
- Memory Protection Unit (MPU)

Bluetooth® Low Energy 5.4[1] (Apollo510B Lite and 510D Lite)

- LE Audio with Auracast™ broadcast audio with LC3 codec
- Direction finding (single antenna) / Long range support
- Periodic advertising with response (PAwR)
- Tx power: Up to +13 dBm output power
- Rx sensitivity: -94/-97/-104 dBm (2/1/0.125 Mbps)
- Supports WLAN and mobile wireless coexistence

Bluetooth Classic (Apollo510D Lite)

- Bluetooth Classic Audio including A2DP and HFP

secureSPOT 3.0 Security Features

- Arm TrustZone technology
- Secure boot
- OTP key storage
- PUF-based identity/sign/verify
- Secure over-the-air (OTA) updates
- Key revocation

Ultra-Low-Power Memory

- Up to 2 MB of non-volatile memory[2] (NVM) for code/data
- 256 kB of TCM and 1.75 MB SSRAM for code/data

Rich Set of Clock Sources

- PLL for precise clocking applications
- 48 MHz and 32.768 kHz Crystal (XTAL) oscillators
- Low Frequency RC (LFRC) oscillator
- High Frequency RC (HFRC) oscillator

Ultra-Low-Power Interface for On- and Off-Chip Sensors

- 12-bit ADC with 11 selectable ADC input channels
- Up to 2.8 MS/s effective continuous, multi-slot sampling rate
- Integrated temperature sensor

Audio Processing

- 1x PDM stereo DMIC interface
- 1x full-duplex multichannel I^2S port

Ultra-Low-Power Flexible Serial Peripherals

- 1x I3C Host interface
- 6x I^2C/SPI mains for peripheral communication
- Full Duplex SPI subordinate for host communication
- MSPI Cfg1: 1x HSPI at 250MT/s + 1 ea QSPI at 96 & 48MT/s
- MSPI Cfg2: 2x OSPI at 250 MT/s + 1x QSPI at 96 MT/s
- 2x UART modules with FIFOs and flow control
- 2x SDIO (v3.0) / eMMC (v4.51)
- 1x USB 2.0 FS/HS device controller

Display Controller

- Memory in Pixel (MiP) display interface with fast-forward
- MIPI DSI 1.2 with two 768 Mbps data lanes (up to 1.5 Gbps)
- QSPI display interface (up to 48 MHz / 96 MT/s DDR)
- Up to 480 x 480 resolution at 60 FPS

graphiqSPOT 2.0 Graphics Features

- 2D/2.5D GPU with vector graphics (VG) acceleration
- Anti-aliasing hardware acceleration
- Rasterizer / full alpha blending / texture mapping
- Texture / frame buffer compression (TSC4, 6, 6A and 12)
- Dithering and radial/conical fill support

Power management

- Operating Voltage: 1.71 V - 2.2 V
- Single inductor multiple outputs (SIMO) buck converter
- Multiple I/O voltages supported

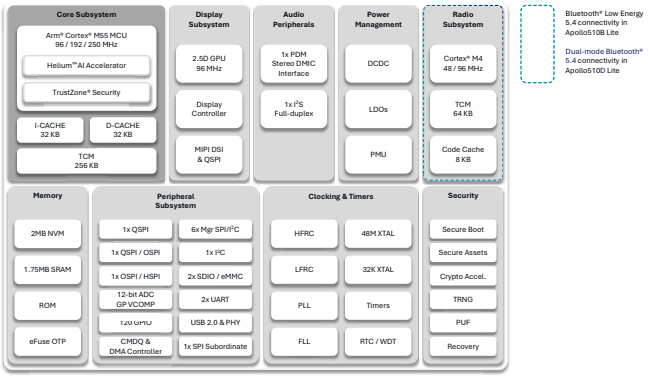
Applications

- Smart watches/bands
- Smart home devices
- Body-worn and ambient AI
- Wireless sensors and industrial edge

Package Options

- 5.3 mm x 5.3 mm x 0.8 mm (max), 13 x 13 BGA (169 pins / 120 GPIO)
- 4.047 mm x 3.948 mm x 0.510 mm (max), 11 x 10 WLCSP (110 pins / 68 GPIO)

1. The *Bluetooth*® word mark and logos are registered trademarks owned by the Bluetooth SIG, Inc. and any use of such marks is under license. Other trademarks and trade names are those of their respective owners.
2. Factory-installed Cortex-M4 firmware reduces the amount of available NVM which varies for each series derivative. The amount of NVM used for each derivative can be viewed in the Cortex-M55 Memory Map



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1. SoC Product Introduction

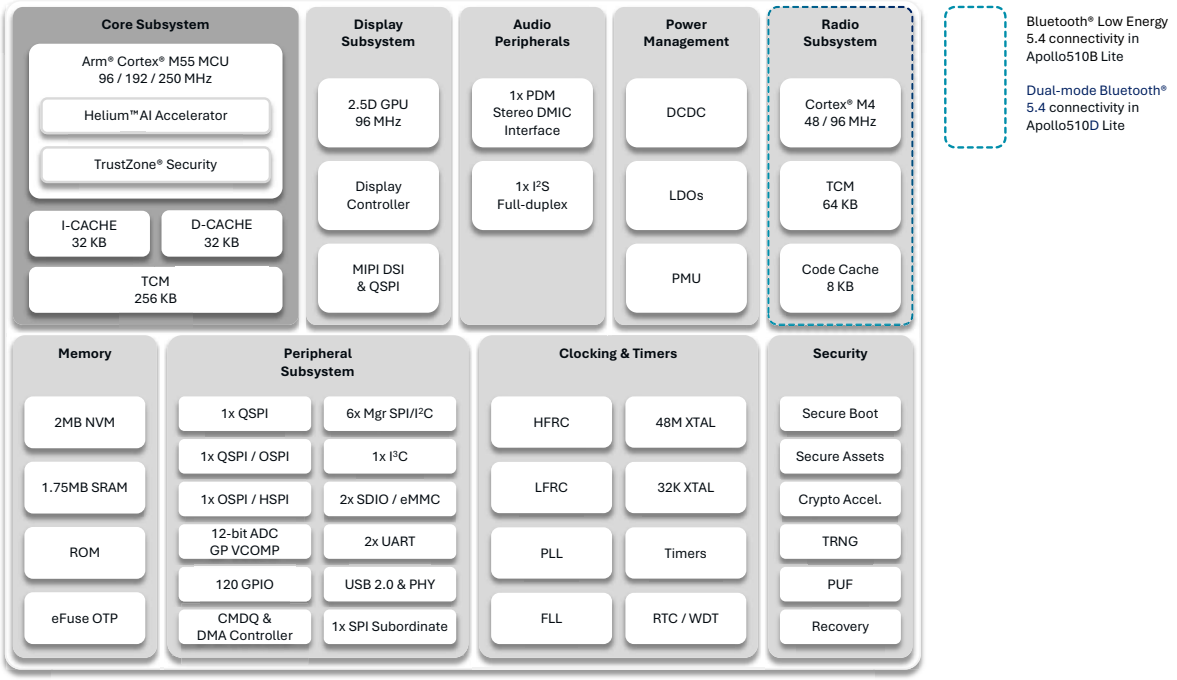

Figure 1. Apollo510 Lite Family SoCs High-Level Block Diagram

1.1 Features

The Apollo510 Lite SoC[1] is an ultra-low power, highly integrated mixed-signal SoC with wireless connectivity (certain derivatives) and designed for battery-powered devices. This series of SoCs delivers the powerful Arm Cortex-M55 processor running at up to 250 MHz, with the Extension Processing Unit which supports M-Profile Vector Extension (MVE) processing (i.e., Helium™ technology) and floating point operations, coupled with the world's lowest power audio and communications processing. The Apollo510 Lite SoC takes the Ambiq Micro's patented Subthreshold Power Optimized Technology (SPOT) Platform to a whole new level of compute power efficiency, setting new industry benchmarks in low power design and high efficiency portable computing.

The Apollo510B Lite SoC and Apollo510D Lite SoC feature a state-of-the-art 2.4 GHz transceiver which is Bluetooth® Low Energy 5.4 compliant. Included are a low-power receiver with excellent sensitivity and selectivity, and a programmable transmitter supporting several output power levels for optimized output power and current consumption.

The Apollo510D Lite SoC further extends connectivity with the addition of an integrated Bluetooth dual-mode radio with Classic support. These SoCs allow for effortless communication and interfacing with various devices, facilitating interoperability and data exchange in diverse endpoints. Additionally, the SoC incorporates advanced security features in secureSPOT® 3.0 with TrustZone® technology, such as secure boot and secure firmware updates, ensuring the integrity and confidentiality of data transmitted and processed by connected devices, making it an ideal choice for secure deployment in various applications.

1. Any references to, or described features of, the "Apollo510 Lite SoC" or the "Apollo510 Lite Series" herein apply to all derivatives of the series. If a feature or function described in this document applies to a specific derivative and/or does not apply to all derivatives, the exception(s) will be noted in the applicable context.

The primary feature differences in the three existing derivatives of the Apollo510 Lite Series are as described in Table 1.

Table 1: Feature and Functional Differences of the Apollo510 Lite Series Derivatives

Feature/Functionality	Apollo510 Lite SoC	Apollo510B Lite SoC	Apollo510D Lite SoC
Bluetooth Low Energy 5.4 Controller	-	✓	✓
Bluetooth Dual Mode (Bluetooth Classic + BLE, BLE only (with or without audio, with or without ANT), 802.15.4)	-	-	✓

The Apollo510 Lite SoC includes features shown in Figure 1 and listed below.

Arm® Cortex®-M55 Application Processor with Helium™ technology:

- Helium (MVE) AI accelerator, up to 8 MACs per cycle
- Up to 250 MHz operating modes
- Helium (MVE) vector integer, floating point
- Arm® TrustZone®[1] enabled hardware
- Scalar half, single, and double-precision floating-point
- Supports TrustZone security extensions
- Integrated 32 kB Instruction Cache and 32 kB Data Cache
- Integrated 256 kB Instruction/Data Tightly Coupled Memory (TCM)
- Memory Protection Unit (MPU)
- Wake-up interrupt controller with 135 interrupts

Bluetooth Low Energy 5.4[2] (Apollo510B Lite and Apollo510D Lite):

- Low Energy Audio with Auracast™ broadcast audio with LC3 codec
- Direction finding (single antenna)
- Advertising extensions
- Long range support
- Periodic advertising with response (PAwR)
- Tx power: Up to +13 dBm output power
- Rx sensitivity: -94 / -97 / -104 dBm (2 / 1 / 0.125 Mbps)
- Supports WLAN and mobile wireless coexistence

Bluetooth Classic (Apollo510D Lite):

- Bluetooth Classic Audio including A2DP and HFP
- Support for Bluetooth Classic + LE or LE only (with or without audio)

secureSPOT 3.0 Security Features:

- Arm TrustZone® technology
- Secure boot
- OTP key storage
- PUF-based identity/sign/verify
- Secure over-the-air (OTA) updates

1. Link to the TF-M documentation: https://www.trustedfirmware.org/projects/tf-m.
2. The *Bluetooth*® word mark and logos are registered trademarks owned by the Bluetooth SIG, Inc. and any use of such marks is under license. Other trademarks and trade names are those of their respective owners.

- Key revocation

Ultra-Low-Power Memory:

- Up to 2 MB[1] of non-volatile memory for code/data
- 256 kB of TCM and 1.75 MB SSRAM for code/data

Ultra-Low-Power Interface for On- and Off-Chip Sensors:

- 12-bit ADC with 11 selectable input channels
  - 10-bit ENOB
  - Up to 2.0 MS/s (12-bit Mode) / 2.8 MS/s (8-bit Mode) effective continuous, multi-slot sampling rate
  - Integrated temperature sensor
- Voltage comparator

Ultra-Low-Power Flexible Serial Peripherals:

- 1x I3C Host Controller with DMA
- 6x I^2C/SPI managers for peripheral communication, DMA and Command Queue
- FD/HD SPI subordinate with DMA support for host communication
- 3x MSPIs[2] supporting SDR/DDR, DMA and Command Queue
  - 1x 2/4/8/16-bit interface up to 250 MT/s
  - 1x 2/4/8-bit interface up to 250 MT/s
  - 1x 2/4-bit interface up to 96 MT/s
- 2x UART modules with 32-location Tx and Rx FIFOs with flow control and DMA support
- 2x SDIO controllers allowing concurrent SDIO (v3.0) / eMMC (v4.51) interface with DMA
- USB 2.0 HS/FS device controller with DMA
- Up to 120 GPIO

Display Controller:

- Memory in Pixel (MiP) display interface with fast-forward
- MIPI DSI 1.2 with 2 data lanes up to 1.5 Gbps (768 Mbps per lane)
- QSPI display interface (up to 48 MHz / 96 MT/s DDR)
- Up to 480 x 480 resolution at 60 FPS[3]
- 1 layer
- Frame buffer decompression

graphiqSPOT 2.0 Graphics Features:

- 2D/2.5D GPU with enhanced Vector Graphics (VG) acceleration
- Anti-aliasing hardware acceleration
- Rasterizer

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1. Factory-installed Cortex-M4 firmware reduces the amount of available NVM which varies for each series derivative. The amount of NVM used for each derivative can be viewed in the Cortex-M55 Memory Map
2. Number of MSPIs and supported data widths are reduced on the WLCSP package.
3. Resulting frame rate at any particular resolution depends upon display interface speed, bus-fabric bandwidth and complexity of the graphics assets and related operations. Typically a resolution of 480 x 480 at 60 frames/second can be supported for most applications.

- Full alpha blending
- Texture mapping
- Texture and frame buffer compression:
  - 4-bit
  - 6-bit (with/without Alpha)
  - 12-bit (with/without Alpha)
- Dithering support
- Radial/conical fill

Audio / Communication Processing:

- 1x PDM stereo DMIC interface
- 1x full-duplex multichannel I^2S port

Rich set of clock sources:

- 250 MHz high precision / low jitter PLL for precise clocking applications
- High frequency XTAL oscillator for BLEC, SYSPLL and other modules (19.2 - 52 MHz)
- 32.768 kHz XTAL oscillator
- High Frequency RC (HFRC) oscillator
- Nominal 900 Hz Low Frequency RC (LFRC) oscillator
- RTC based on Ambiq's AM08X5/18X5 families
  - Wake from RTC capability

Power Management:

- Operating ranges:
  - Voltage: 1.71 V - 2.2 V[1]
- Single Inductor Multiple Outputs (SIMO) Buck Converter
- Multiple I/O voltage domains supported (independent voltage rails)

Package(s):

- 5.3 mm x 5.3 mm x 0.8(max) mm, 13 x 13 BGA (169 pins /120 GPIO)
- 4.047 mm x 3.948 mm x 0.510(max) mm, 11 x 10 WLCSP (110 pins / 68 GPIO)

1. The RF subsystem's supplies and the MIPI PHY require a 1.8 V supply, so systems operating higher than 2.2 V require additional external regulator(s) if these functions are to be used.

1.2 Functional Overview

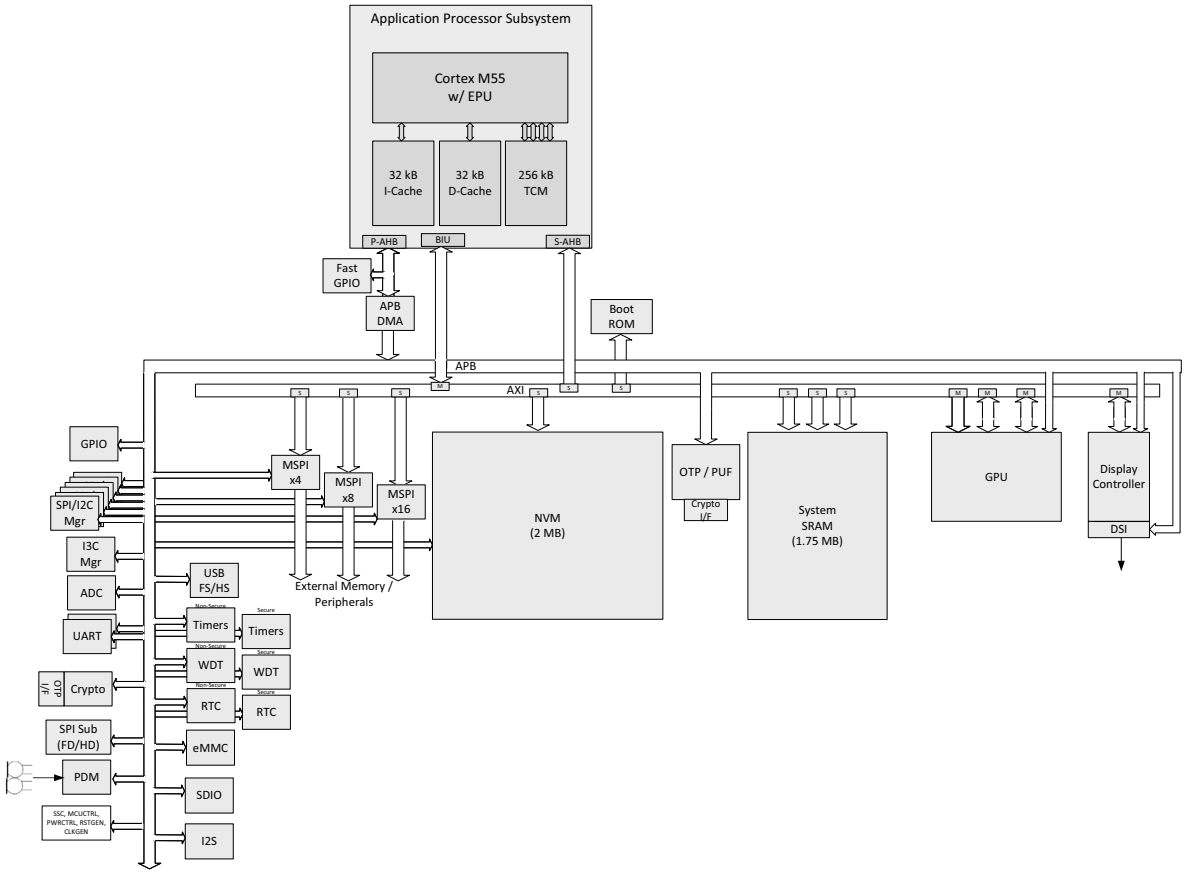

Figure 2. Apollo510 Lite SoC Detailed Block Diagram

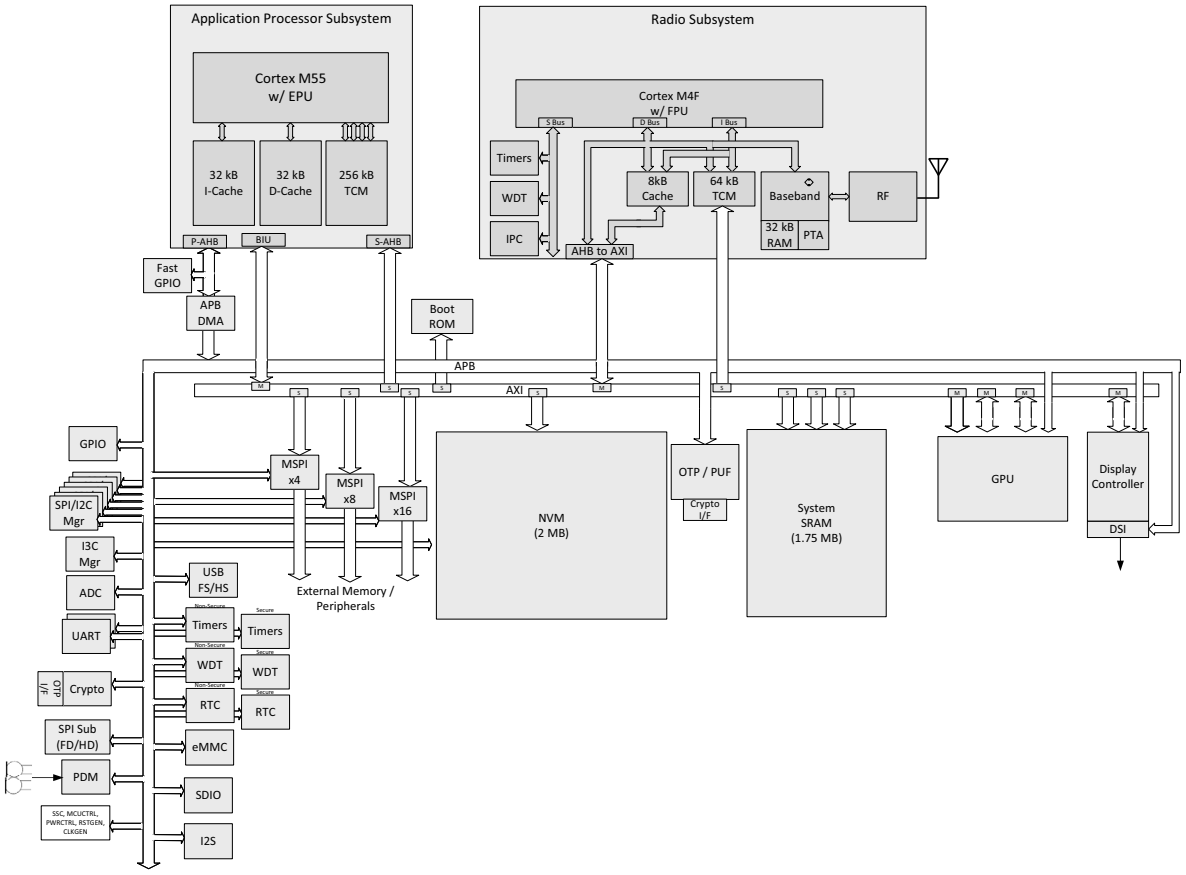

Figure 3. Apollo510B Lite SoC / Apollo510D Lite SoC Detailed Block Diagram

The ultra-low power Apollo510 Lite SoC, shown in Figure 2 and Figure 3, provides an ideal solution for battery-powered applications supporting near- to far-field audio processing. In a typical system, the SoC serves as an applications processor with fully integrated audio subsystem. The Apollo510 Lite SoC includes an extensive set of digital and analog peripheral interfaces with integrated ADCs and digital sensor processing using the integrated serial manager ports. The Cortex-M55 core with Helium™ technology, also known as the M-Profile Vector Extension (MVE), integrated in the Apollo510 Lite SoC is capable of running complex data analysis and sensor fusion algorithms to process the sensor data and orchestrate complex audio processing signal flows. The Cortex-M55 core leverages a broad development and support ecosystem to accelerate time-to-market for application and product deployment.

In other configurations, a host processor can communicate or share data with the Apollo510 Lite SoC over its serial subordinate port using its SPI interface or by using the I^2S audio streaming interface module, both of which support full duplex data transfer. With unprecedented energy efficiency for sensor conversion, audio processing and data analysis, the SoC enables months and years of battery life for products only achieving days or months of battery life today. Similarly the device enables the use of significantly complex algorithmic processing due to its industry leading low active mode power. By using the Apollo510 Lite SoC, artificial intelligence at the portable edge (Edge AI) is truly brought to life.

The Apollo510 Lite SoC supports various operating modes to maximize energy efficiency depending on the workload demand. For extremely power-sensitive workloads, it supports a low power operating mode leveraging Ambiq Micro's patented SPOT technology to achieve industry leading energy efficiency. For timing critical or higher MIPs workloads, the device supports high performance operating modes through

Ambiq Micro's TurboSPOT technology. The TurboSPOT technology enables high performance while still maintaining extremely high energy efficiency operation. The device also supports secure boot using Ambiq's SecureSPOT technology enabling applications to establish and maintain a root of trust from boot to execution.

The Apollo510 Lite SoC brings enhanced display and user interface capabilities with a rich set graphics features. A powerful 2.5D graphics controller with vector graphics acceleration enables a rich UI experience without compromise on power. Texture and frame buffer compression (4/6/12-bit) is supported to minimize storage and bandwidth requirements.

A rich set of sensor peripherals enable the monitoring of several sensors. An integrated temperature sensor enables the measurement of ambient temperature. A scalable ultra-low power Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) monitors the temperature sensor, several internal voltages, and up to eight external sensor signals. The General Purpose ADC is uniquely tuned for minimum power with a configurable measurement mode that does not require MCU intervention. In addition to integrated analog sensor peripherals, I3C/I2C/SPI manager ports and/or UART ports enables the MCU to communicate with external sensors that have digital outputs.

The Apollo510 Lite SoC integrates an audio subsystem supporting 1x stereo PDM microphones and 1x I2S manager/subordinate full duplex support. Additionally, ultra low power wake on voice and wake on keyword is supported.

For higher bandwidth peripherals, the Apollo510 Lite SoC supports one Multi-bit SPI (MSPI1) controller for 1-bit, 2-bit and 4-bit data, one MSPI (MSPI2) for 1-bit, 2-bit, 4-bit and 8-bit data, and one MSPI (MSPI0) capable of up to 16-bit data (three MSPI controllers total).

NOTE
MSPI1 is not pinned out and MSPI2 is limited to a maximum data width of 4-bit (Quad SPI) on the WLCSP package of Apollo510 Lite SoC. MSPI0 supports 16-bit data width, same as on the BGA package, but is limited to a maximum of 8-bit data width when used concurrently with MSPI2.

The Apollo510 Lite SoC also includes a set of timing peripherals and an RTC which is based on Ambiq's AM08XX and AM18XX Real-Time Clock (RTC) families. The general purpose Timer/Counter Module (CTIMER), 32-bit System Timer (STIMER), and the RTC may be driven independently by one of three different clock sources: a low frequency RC oscillator, a high frequency RC oscillator, and a 32.768 kHz crystal (XTAL) oscillator. These clock sources use the proprietary advanced calibration techniques developed for the AM08XX and AM18XX products that achieve XTAL-like accuracy with RC-like power.

Additionally, the Apollo510 Lite SoC includes clock reliability functions first offered in the AM08XX and AM18XX products. For example, the RTC can automatically switch from an XTAL source to an RC source in the event of an XTAL failure.

The Apollo510 Lite SoC supports optimized PWM pattern generation for complex control operation.

To facilitate development and debug, the Apollo510 Lite SoC is supported by a complete suite of standard software development tools. Ambiq Micro provides drivers for all peripherals along with basic application code to shorten development times. Software debug on the Cortex-M55 is facilitated by the addition of an Instrumentation Trace Macrocell (ITM), Embedded Trace Macrocell (ETM) and a Trace Port Interface Unit (TPIU). The debug functions are accessible via Serial Wire Debugger (SWD).

1.3 Functional Differences between BGA and WLCSP Packages

This section highlights the differences between the BGA and WLCSP packages of the Apollo510 Lite SoC due to the reduced pinout of the WLCSP package.

1.3.1 GPIO

Some GPIO on the BGA are not brought out on the WLCSP. Those GPIO are GPIO40-42, 47-58, 78, 80, 82-106, 109 and 111-119, for a total of 52 GPIO not available on the WLCSP. See the Apollo510 Lite SoC Pin Mapping table in the GPIO section for the GPIO pads offered on the two packages and which VDDHn power rail that each pad uses.

1.3.2 MSPI

MSPI0:

- Only CE1 is pinned out and available as a chip select on the WLCSP package.

MSPI1:

- None of the MSPI1 pins are pinned out on the WLCSP package.

MSPI2:

- Only CE0 is pinned out and available as a chip select on the WLCSP package.
- The MSPI2_8 signal is not available as a dedicated clock line so the MSPI2_4 data line must be used for the clock on the WLCSP package, which limits MSPI2's maximum data width to 4-bits (Quad SPI).
- The lower-speed GPIO with MSPI2 4-bit data width capability is not pinned out on the WLCSP package. Because of this and since MSPI0 and MSPI2 share high-speed pins, *concurrent* MSPI0 and MSPI2 operation is limited to 8-bit data width for MSPI0.

1.3.3 Display Subsystem

The MIPI DBI-Type B / Type C Display Bus Interface and the MIPI DPI-2 interface are not offered on the WLCSP package.

2. CPU Subsystem

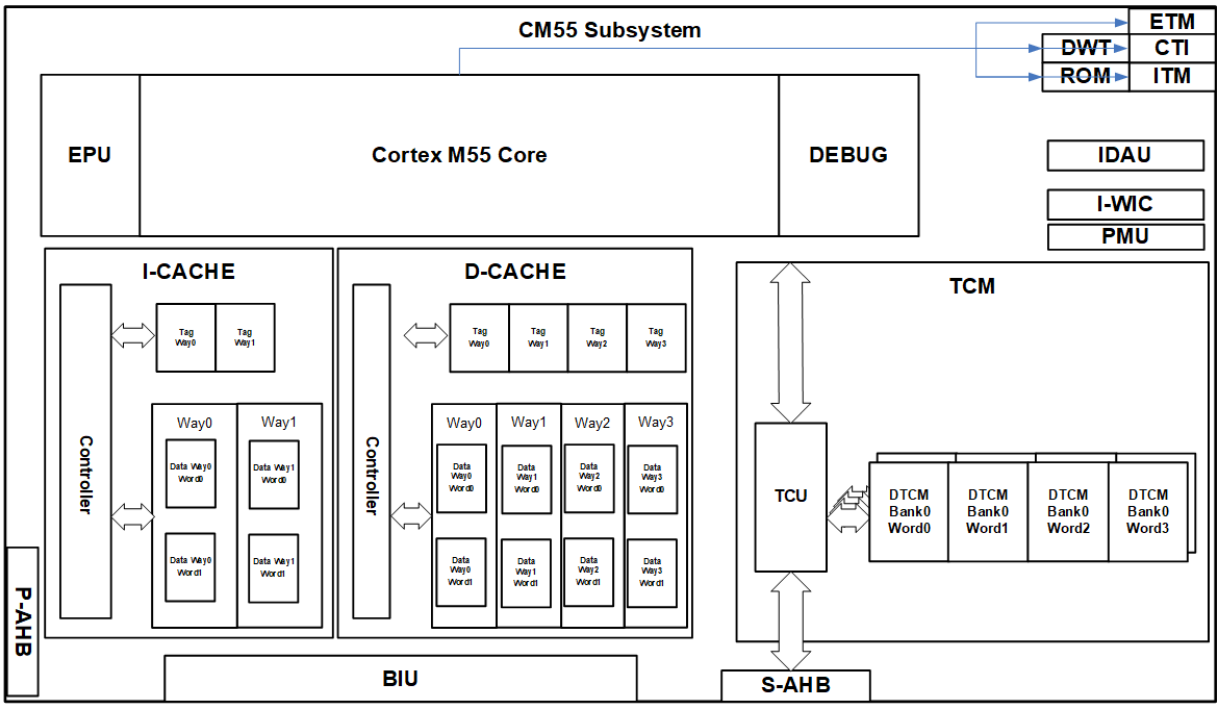

Figure 4. Apollo510 Lite SoC CPU Subsystem Block Diagram

2.1 Features

The CPU subsystem (or CPU complex) includes features as shown in Figure 4 and is composed of an Arm Cortex-M55 CPU with Helium technology, instruction and data caching, instruction and data tightly coupled memory, interrupt and debug logic as well as the associated power management control for the subsystem. The subsystem has the following features:

- Cortex-M55 with Helium technology
  - Half-Precision, Single-Precision and Double Precision Floating Point
  - Vector Processing supporting integer, half-precision and single-precision vector arithmetic
- Arm®v8.1-M ISA with DSP Extensions
- TrustZone® technology support
- Operating Modes
  - 96 MHz Low Power Mode
  - 192 MHz / 250 MHz High Performance Mode
- Internal WIC (iWIC) supported
- Memory Protection Unit: 16 non-secure and 16 secure memory regions
- Security attribution Unit: 8 regions
- Debug
  - Embedded Trace Macrocell (ETM)
  - 8x data watchpoint comparators and 8x breakpoint comparators
  - ITM/DWT supported
- CPU Power Management block
- 32 kB Instruction Cache / 32 kB Data Cache
- 256 kB Instruction/Data TCM

NOTE

Limitations of DMA operations include the following:

- Transferring between memory/NVM (TCM, SSRAM, NVM) source and destination is not supported as the APBDMA does not have the capability to transfer from memory to memory. When TCM is the source of the DMA transfer, the transfer should target a peripheral.
- A DMA operation cannot be performed to or from TCM when the CPU is in deep sleep or the TCM location is powered down.
- A DMA transfer must not cross a TCM 4 kB boundary.

2.2 Functional Overview

At the center of the Apollo510 Lite SoC is a 32-bit Arm Cortex-M55 core with floating point and vector processing (Helium technology) option. This implementation of the ArmV8.1-M architecture offers highly efficient processing in a very low power design. The Arm M DAP enables debugging access via a Serial Wire Interface from outside of the MCU which allows access to all of the memory, processors and peripheral devices of the SoC. The Apollo510 Lite SoC supports the Cortex-M55 with Helium technology enabling high efficiency compute non-secure processing support. TrustZone ISA extensions are supported to enable secure computing.

The CPU complex has 32 kB of instruction caching and 32 kB of data caching, as well as 256 kB of TCM. In addition, the CPU has access to 1.75 MB of total shared system SRAM, 2 MB of non-volatile memory[1] and up to 3 external memory interfaces ranging in size from 64 MB to 256 MB. All of the memory is memory mapped and accessible by the CPU. All of the memory accesses are qualified based on the memory protection attributes (enforced within the Cortex-M55) and the system memory protection attributes (enforced within the system memory controllers).

The Cortex-M55 processor supports the Arm®v8.1-M Protected Memory System Architecture (PMSA) that provides programmable support for memory protection using a number of software controllable regions. Memory regions can be programmed to generate faults when accessed inappropriately by unprivileged software reducing the scope of incorrectly written application code. The architecture includes fault status registers to allow an exception handler to determine the source of the fault and to apply corrective action or notify the system.

Reference the “Arm Cortex-M55 Processor Technical Reference Manual” for more details.

2.3 Memory Protection Unit (MPU)

The Apollo510 Lite SoC includes an MPU which is a core component for memory protection. The Cortex-M55 processor supports the Arm®v8.1-M Protected Memory System Architecture (PMSA). With the Security Extension, the Cortex-M55 supports both an MPU for the non-secure domain and an S-MPU for the secure domain.

The MPU is an optional component and, when implemented, provides full support for:

- Protection regions
- Access permissions
- Exporting memory attributes to the system

1. Factory-installed Cortex-M4 firmware reduces the amount of available NVM which varies for each series derivative. The amount of NVM used for each derivative can be viewed in the Cortex-M55 Memory Map

MPU mismatches and permission violations invoke the MemManage handler. See the “ArmV8.1-M Architecture Reference Manual” for more information.

The MPU can be used to enforce privilege rules, separate processes and manage memory attributes. The Apollo510 Lite SoC supports up to 16 memory regions and the S-MCU supports up to 16 *secure* memory regions.

2.4 Power Management Overview

Power management is partitioned into several components across the Apollo510 Lite SoC. For the CPU complex, a dedicated finite-state machine controls the transitions of the CPU between power modes. When moving from Active Mode to Deep Sleep Mode, the CPU-PMU manages the state-retention capability of the registers within the Cortex-M55 core and also handshakes with the central power management controller to appropriately handle the voltage rails to the CPU complex. Once in Deep Sleep Mode, the CPU-PMU, in conjunction with the Wake-Up Interrupt Controller, waits for a wakeup event. When the event is observed, the CPU-PMU begins the power restoration process by handshaking with the central power management controller to adjust the voltage rails to the CPU complex and initiate the restoration of the CPU register state. The Cortex-M55 is then returned to active mode once all state is ready.

2.4.1 Cortex-M55 Power Modes

The Arm Cortex-M55 supports power modes as listed in Table 2.

Table 2: Arm Cortex-M55 Power Modes

Ambiq M55 Power Mode	Arm M55 Power Mode
HP Active	Active
Active	
Sleep	ON, clock off
Deep Sleep	Retention
Off	Off

In addition to the above Arm-defined modes, the Apollo510 Lite SoC supports system level power modes which are defined in the Power Management chapter. See section “Program Control of Power Management” on page 46 which describes programmatic control of power mode transitioning via the MCUPERFREQ register and other module/processor-specific registers in the PWRCTRL register set.

2.4.1.1 High Performance Mode

The Apollo510 Lite SoC supports the Ambiq TurboSPOT™ which enables a higher frequency operating mode (HP Mode). In this mode, the Cortex-M55 and all closely coupled memory run at an elevated frequency. All of the non-debug Arm clocks (FCLK, HCLK) also operate at the elevated frequency level. All peripherals are maintained at the nominal frequency level during burst. This mode is entered and exited under software direction but transitions are completely handled in hardware.

This is not a standard Arm-defined power mode. From the Arm core, this mode is treated similarly to “Active Mode”.

2.4.1.2 Active Mode

In the Active Mode, the Cortex-M55 core is powered up, clocks are active, and instructions are being executed. In this mode, the Cortex-M55 expects all (enabled) devices attached to the interfaces to be powered and clocked for normal access. All of the non-debug Arm clocks (FCLK, HCLK) are active in this state.

To transition from the Active Mode to any of the lower-power modes, a specific sequence of instructions is executed on the Cortex-M55 core. First, specific bits in the Armv8-M System Control Register must be set to determine the mode to enter. See the Armv8-M Architecture Reference Manual for more details.

After the SCR is setup, code can enter the low-power states using one of the three following methods:

- Execute a Wait-For-Interrupt (WFI) instruction.
- Execute a Wait-For-Event (WFE) instruction.
- Set the SLEEPONEXIT bit of the SCR such that the exit from an ISR will automatically return to a sleep state.

The Cortex-M55 will enter a low-power mode after one of these are performed (assuming all conditions are met) and remain there until some event causes the core to return to Active Mode. The possible reasons to return to Active Mode are:

- A reset
- An enabled Interrupt is received by the NVIC
- An event is received by the NVIC
- A debug event is received from the DAP

2.4.1.3 Sleep Mode

In Sleep Mode, the Cortex-M55 is powered up, but the clocks (HCLK, FCLK) are gated. The power supply is still applied to the Cortex-M55 logic such that it can immediately become active on a wakeup event and begin executing instructions.

2.4.1.4 Deep Sleep Mode

In Deep Sleep Mode, the Cortex-M55 enters SRPG mode where the main power is removed, but the flops retain their state. The clocks are not active, and the MCU clock sources for HCLK and FCLK can be deactivated. To facilitate the removal of the source supply and entry into SRPG mode, the Cortex-M55 will handshake with the Wake-up Interrupt Controller and Power Management Unit and set up the possible wakeup conditions.

Note that on the Apollo510 Lite Series SoCs, a new deep sleep mode, SYS Deep Sleep Mode 3, has been added where minimal SRAM memory is retained as needed for software to resume operation. See Section 4.2.1.4 on page 44.

2.5 Debug

The Apollo510 Lite SoC supports several debug features to facilitate software development, profiling and analysis. Standard Serial Wire Debug (SWD) interface is supported along with 1-bit and 4-bit trace data port and optional Serial Wire Output (SWO).

The CPU debug components in the Apollo510 Lite SoC support the following features:

- Secure and Non-Secure Debugging
- Embedded Trace Macrocell (ETM)
- Instrumentation Trace Macrocell (ITM) supporting instrumentation tracing and trace port via Serial Wire Output (SWO)
- Trace Port Interface Unit (TPIU)
- 8x Data Watchpoint and Trace (DWT)

- 8x Breakpoint Unit (BPU)
- Hardware fault reporting
- Serial Wire Debug (SWD)
- Performance Monitoring Unit (PMU)

2.5.1 Embedded Trace Macrocell (ETM)

The Apollo510 Lite SoC supports hardware instruction tracing via an Embedded Trace Macrocell (ETM). The ETM stream is accessible via APB or TPIU. Note that while ETM 4.5 is capable of supporting data tracing as well as instruction tracing, data tracing was not implemented in the ETM-M55. However, data-tracing facilities are available through the DWT.

2.5.2 Instrumentation Trace Macrocell (ITM)

For system trace the processor integrates an Instrumentation Trace Macrocell (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system events these generate, a Serial Wire Viewer (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

2.5.3 Trace Port Interface Unit (TPIU)

The Apollo510 Lite SoC includes a Cortex-M55 Trace Port Interface Units (TPIU) which can take input from the CPU ITM or ETM. It is an Arm IP component that supports a 1-bit or 4-bit trace data port and Serial Wire Output (SWO). It can act as a bridge between the on-chip trace data from the ITM and the single pin supporting the Serial Wire Viewer Protocol, as well as support the ETM trace output. The TPIU includes a Trace Output Serializer that can format and send the SWV protocol in either a Manchester encoded form or as a standard UART stream.

NOTE
For ETM instruction tracing, Arm recommends the 4-bit trace data port with the TPIU input frequency matching the maximum CPU frequency (250 MHz) for TPIU TRACECLKIN. Note that only GPIO0 to GPIO4 or GPIO35 to GPIO39 can be used as the TRACE port for clock frequencies above 96 MHz.

2.5.4 Serial Wire Debug (SWD)

An external debugger can be connected to the MCU using the Arm Serial Wire Debug (SWD) interface. The SWD interface is a 2-wire interface that is supported by a variety of off-the-shelf commercial debuggers, enabling customers to utilize their development environment of choice.

2.5.5 Performance Monitoring Unit (PMU)

The Performance Monitoring Unit (PMU) is a powerful tool used for code profiling and optimization and provides the following capabilities:

- Collect real-time data to fine-tune applications, maximizing efficiency and performance on the Cortex-M55 core.
- Track memory usage and identify system inefficiencies, enhancing responsiveness and minimizing slow memory accesses.

- Optimize AI and digital signal processing by monitoring vector unit utilization and enhancing throughput on complex tasks.
- Gather detailed data on execution patterns, helping identify and resolve bottlenecks faster.

2.5.6 Data Watchpoint and Trace (DWT)

The Data Watchpoint and Trace (DWT) of the Cortex-M55 (ArmV8-M) includes watchpoints, data value watchpoints, and trace control signaling which can be used to control the ETM and CTI, performance profiling and more. It does not perform tracing of all data addresses issued by the processor.

See the Arm Cortex-M55 Technical Reference Manual, section 17.1 and ArmV8-M Architecture Reference Manual, section D1.2.63 for more details.

2.5.7 Breakpoint Unit (BPU)

The BPU is configured with four instruction address comparators. Each comparator supports breakpoint functionality on all instructions that are fetched across the entire address range in which code is located. If invasive debug is not enabled for a security mode, then debug events associated with breakpoints in that mode are blocked.

2.5.8 Faulting Address Trapping Hardware

The Apollo510 Lite SoC offers an optional facility for trapping the address associated with bus faults occurring on any of the three AMBA AHB buses on the chip. This facility must be specifically enabled so that energy is not wasted when one is not actively debugging. The Cortex-M55 core provides bus fault information using the Configurable Fault Status Register that can be configured for usage fault, bus fault and memory management fault reporting. The Auxiliary Fault Status Register provides additional information on the types and causes of faults. The Bus Fault Address Register and the MemManage Fault Address Register capture the memory address that caused one of these faults.

2.5.9 PPB/EPPB Interfaces

The ITM, DWT, BPU, CTI and ETM programming interfaces are provided through the Cortex-M55 private peripheral bus (PPB). The system TPIU is provided on the external private peripheral bus (EPPB).

2.6 Additional Information

Please refer to the MCUCTRL registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

3. Memory Subsystem

3.1 Features

The memory for the CPU subsystem consists of the following features.

- 2-way set associative instruction cache
- 4-way set associative data cache
- Tightly-coupled memory
- NVM interface
- System SRAM interface

3.2 Functional Overview

The instruction cache for the CPU subsystem caches all instruction accesses to the code region of the memory map. On the Apollo510 Lite SoC, this memory includes internal and external non-volatile memory.

The instruction cache has the following features:

- 32 kB capacity
- 2-way set-associative
- 32-byte line size

The data cache has the following features:

- 32 kB capacity
- 4-way set-associative
- 32-byte line size
- Write-back and write-through cacheable
- Read-allocate and no read-allocate
- Write-allocate and no write-allocate
- Transient and non-transient. Clean cache lines that are associated with transient memory are prioritized for eviction over lines that are associated with non-transient memory

The store buffer has five 64-bit entries and has merging capabilities. If a previous write access has updated an entry, other write accesses on the same double-word can merge into this entry.

The TCM is 256 kB in size and provides zero wait-state data memory access to the CPU. The TCM is a low power / low latency memory that can be used for data and instruction accesses.

The Shared SRAM (SSRAM) is accessible via the SRAM region. The SSRAM shared system memory is composed of 2 power domains: 1024 kB domain and 768 kB domain. Access to this memory region incurs 8 or more cycle wait-states, depending on the CPU operating mode.

The CPU sub-system includes a boot ROM which is the initial boot memory for the system. The boot ROM initiates the secure boot flow, if enabled, as well as other primitive/critical helper functions to facilitate accesses such as NVM programming.

NOTE
MRAM magnetic immunity guidelines are provided to assist with end product design - see the *“Design Guidelines for Magnetic Immunity”*, document number A-SOCAP4-ANGA01EN, as well as the *“Apollo5 MRAM Recovery Users Guide”*, document number A-SOCAP5-UGGA01EN, in the Ambiq Content portal - https://contentportal.ambiq.com.

ERRATUM NOTICE

The option to use data line D4, MSPIn_4, as the clock output line for an MSPI is not supported by the Boot ROM of Apollo510 Lite Series SoCs. The standard clock line, MSPIn_8, must be used by the Boot ROM, i.e., for the purpose of recovering MRAM.

Note that the MSPI2_8 clock output is not pinned out on the WLCSP package of Apollo510 Lite Series SoCs requiring the use of the MSPI2_4 pin to clock MSPI2, which is enabled by setting the MSPI2_PADOUTEN_CLKOND4 bit. However, since this clock line configuration is not supported by the BootROM, MSPI2 cannot be used for recovering MRAM. Only MSPI0 is available for use in that scenario on the WLCSP package.

3.3 Interrupts

Within the SoC, multiple peripherals can generate interrupts. In some cases, a single peripheral may be able to generate multiple different interrupts. Each interrupt signal generated by a peripheral is connected to one of the processing cores. For interrupts that route back to the Cortex-M55 core, these can be routed to two places. First, the interrupts are connected to the Nested Vectored Interrupt Controller, NVIC, in the core. This connection provides the standard changes to program flow associated with interrupt processing. Additionally, they are connected to the WIC outside of the core, allowing the interrupt sources to wake the Cortex-M55 core when it is in a deep sleep (SRPG) mode.

For details on the interrupt model of the Cortex-M55, please see the “Cortex-M55 Devices Generic User Guide.” The VTOR register in the System Control Block (SCB) determines the starting address of the vector table.

In the Apollo510 Lite SoC implementation with the Security Extension, the VTOR is banked so there is a VTOR_S and a VTOR_NS. The initial values of VTOR_S and VTOR_NS are system design specific. The vector table used depends on the target state of the exception. For exceptions targeting the Secure state, VTOR_S is used. For exceptions targeting the Non-secure state, VTOR_NS is used.

Note that for non-secure interrupts, the value in the secure vector table will be an invalid address to generate an exception as this is an error condition (which could be the non-secure address as jumping to it would be a security error). Conversely, for secure-interrupts, the value in the non-secure table will be an invalid address for non-secure code (could be the secure address as this would generate a security error). Banked interrupts means there are secure and non-secure versions of this interrupt. Therefore the vector values in each of the secure and non-secure versions are valid, and should be different (one secure and one non-secure).

3.3.1 Vector Table for Apollo510 Lite SoC

In the Apollo510 Lite SoC implementation with the Security Extension, the VTOR is banked so there is a VTOR_S and a VTOR_NS. The initial values of VTOR_S and VTOR_NS are system design specific. The vector table used depends on the target state of the exception. For exceptions targeting the secure state, VTOR_S is used. For exceptions targeting the non-secure state, VTOR_NS is used.

Note that for non-secure interrupts, the value in the secure vector table will be an invalid address to generate an exception as this is an error condition. Conversely, for secure-interrupts, the value in the non-secure table will be an invalid address for non-secure code. Banked interrupts mean there are secure and non-secure versions of this interrupt. Therefore the vector values in each of the secure and non-secure versions are valid, and should be different (one secure and one non-secure).

Table 3 represents the Cortex-M55 Vector Table for the Apollo510 Lite SoC.

Table 3: Apollo510 Lite SoC Cortex-M55 Vector Table

Exception Number	IRQ	Offset	Vector	Description
154	138	0x268	IRQ138	Reserved
153	137	0x264	IRQ137	Reserved
152	136	0x260	IRQ136	Reserved
151	135	0x25C	IRQ135	Reserved
150	134	0x258	IRQ134	OTP
149	133	0x254	IRQ133	FP Exception[1]
145 - 148	129 - 132	0x244 - 0x250	IRQ129 - 132	Reserved
141 - 144	125 - 128	0x234 - 0x240	IRQ 125 - 128	GPIO8 - 11: MCUN1INTn (n = 0 to 3)
125 - 140	109 - 124	0x1F4 - 0x230	IRQ109 - 124	TIMER2 0 - 15
124	108	0x1F0	IRQ108	STIMER2 Capture/Overflow
116 - 123	100 - 107	0x1D0 - 0x1EC	IRQ100 - 107	STIMER2 Compare[0:7]
115	99	0x1CC	IRQ99	IOSFD1 SPI Subordinate Register Access
114	98	0x1C8	IRQ98	IOSFD1 SPI Subordinate
113	97	0x1C4	IRQ97	IOSFD0 SPI Subordinate Register Access
112	96	0x1C0	IRQ96	IOSFD0 SPI Subordinate
108 - 111	92 - 95	0x1B0 - 0x1BC	IRQ92 - IRQ95	SW INT[3:0]
107	91	0x1AC	IRQ91	Reserved
106	90	0x1A8	IRQ90	Reserved
105	89	0x1A4	IRQ89	Reserved
104	88	0x1A0	IRQ88	Reserved
103	87	0x19C	IRQ87	Reserved
102	86	0x198	IRQ86	Reserved
101	85	0x194	IRQ85	I3C0
100	84	0x190	IRQ84	SDIO1
88 - 99	72 - 83	0x160 - 0x18C	IRQ72 - IRQ83	Reserved
87	71	0x15C	IRQ71	Secure Counter/Timers (combined - also see IRQ 67-70)
86	70	0x158	IRQ70	Secure Timer 3
85	69	0x154	IRQ69	Secure Timer 2
84	68	0x150	IRQ68	Secure Timer 1
83	67	0x14C	IRQ67	Secure Timer 0
82	66	0x148	IRQ66	Reserved
81	65	0x144	IRQ65	Reserved
80	64	0x140	IRQ64	Reserved
76 - 79	60 - 63	0x130 - 0x13C	IRQ60 - IRQ63	Reserved

Table 3: Apollo510 Lite SoC Cortex-M55 Vector Table

Exception Number	IRQ	Offset	Vector	Description
72 - 75	56 - 59	0x120 - 0x12C	IRQ56 - IRQ59	GPIO Group 0 - 3: MCUN0INTn (n = 0 to 3)
71	55	0x11C	IRQ55	Reserved
70	54	0x118	IRQ54	Reserved
69	53	0x114	IRQ53	Reserved
68	52	0x110	IRQ52	Reserved
67	51	0x10C	IRQ51	Reserved
66	50	0x108	IRQ50	Reserved
65	49	0x104	IRQ49	Reserved
64	48	0x100	IRQ48	PDM0
63	47	0xFC	IRQ47	Reserved
62	46	0xF8	IRQ46	Reserved
61	45	0xF4	IRQ45	Reserved
60	44	0xF0	IRQ44	I2S0
59	43	0xEC	IRQ43	Reserved
58	42	0xE8	IRQ42	Reserved
57	41	0xE4	IRQ41	RTC2
56	40	0xE0	IRQ40	Secure STIMER Capture/Overflow
48 - 55	32 - 39	0xC0 - 0xDC	IRQ32 - IRQ39	Secure STIMER Compare[0:7]
47	31	0xBC	IRQ31	WDT2
46	30	0xB8	IRQ30	DSI
45	29	0xB4	IRQ29	Display
44	28	0xB0	IRQ28	Graphics
43	27	0xAC	IRQ27	USB
42	26	0xA8	IRQ26	SDIO0
41	25	0xA4	IRQ25	Reserved
40	24	0xA0	IRQ24	Secure CRYPTO
39	23	0x9C	IRQ23	Secure Clock Control
38	22	0x98	IRQ22	MSPI2
37	21	0x94	IRQ21	MSPI1
36	20	0x90	IRQ20	MSPI0
35	19	0x8C	IRQ19	GPADC
34	18	0x88	IRQ18	IPC (Cortex-M55) Error
33	17	0x84	IRQ17	IPC (Cortex-M55) Pending Message
32	16	0x80	IRQ16	UART1
31	15	0x7C	IRQ15	UART0
30	14	0x78	IRQ14	Counter/Timers (combined - also see IRQ 109 - 124)

Table 3: Apollo510 Lite SoC Cortex-M55 Vector Table

Exception Number	IRQ	Offset	Vector	Description
29	13	0x74	IRQ13	Reserved
28	12	0x70	IRQ12	Reserved
27	11	0x6C	IRQ11	I^2C/SPI Manager5
26	10	0x68	IRQ10	I^2C/SPI Manager4
25	9	0x64	IRQ9	I^2C/SPI Manager3
24	8	0x60	IRQ8	I^2C/SPI Manager2
23	7	0x5C	IRQ7	I^2C/SPI Manager1
22	6	0x58	IRQ6	I^2C/SPI Manager0
21	5	0x54	IRQ5	Reserved
20	4	0x50	IRQ4	Reserved
19	3	0x4C	IRQ3	Voltage Comparator
18	2	0x48	IRQ2	Secure RTC
17	1	0x44	IRQ1	Secure Watchdog Timer
16	0	0x40	IRQ0	Brownout Detection
15	-1	0x3C	Systick(_S)	System Tick
14	-2	0x38	PendSV(_S)	
13	-	0x34	Reserved	
12	-4	0x30	DebugMonitor	
11	-5	0x2C	SVCall(_S)	
10	-	0x28	Reserved	
9	-	0x24		
8	-	0x20		
7	-9	0x1C	SecureFault_S	Secure Fault
6	-10	0x18	UsageFault_S	Usage Fault
5	-11	0x14	BusFault_S	Bus Fault
4	-12	0x10	MemoryManage_S	Memory Management Fault
3	-13	0xC	HardFault_S	Hard Fault
2	-14	0x8	NMI_S	
1	-	0x4	Reset	
		0x0	Initial SP	

1. Floating point exception interrupt is raised when one of six possible FP errors is detected. The FPSCR register must be interrogated to determine the source(s) of the interrupt. Note that the interrupt is not banked (nor is FPSCR), so the interrupt must be reassigned secure if a FP secure context is created. (The FPDSCR is banked).

3.3.2 GPIO Extension

The Apollo510 Lite SoC supports up to 120 GPIOs. Interrupt mapping is in groups of 32 GPIOs. There are two sets of groups allowing for finer granularity of GPIO interrupt handling. Each interrupt is enabled, disabled, cleared or set with a standard set of interrupt registers - REG_GPIO_MCUN0INTnEN, REG_GPIO_MCUN0INTnSTAT, REG_GPIO_MCUN0INTnCLR and REG_GPIO_MCUN0INTnSET, where n = 0 to 3 for GPIO pads 0 to 31, 32 to 63, 64 to 95 and 96 to 119, respectively. The N0 designation in these registers indicates that these are interrupt register set 0. A duplicate set of registers, with a designation N1, is available and these registers are similarly named REG_GPIO_MCUN1INTnEN, REG_GPIO_MCUN1INTnSTAT, REG_GPIO_MCUN1INTnCLR and REG_GPIO_MCUN1INTnSET. The purpose of this dual set of registers is to enable segregation of an interrupt, or a small set of interrupts, which may have higher importance and thus should be handled at a higher priority level and/or with minimal latency.

3.4 Memory Maps

Table 4 shows the memory map for the Arm Cortex-M55 CPU used by the Apollo510 Lite Series SoCs.

> NOTE
>
> TrustZone documentation will be available at a later date.

Table 4: Cortex-M55 CPU Memory Map

Type	Address Range	Name	Executable	Description
Code	0x00000000 - 0x003BFFFF	Reserved	X	Reserved
	0x003C0000 - 0x003CFFFF	RS TCM RAM	Y	Radio subsystem TCM RAM (64 kB)
	0x003D0000 - 0x003FFFFF	Reserved	X	Reserved
	0x00400000 - 0x005FBFFF (510 Lite) 0x00400000 - 0x005B7FFF (510B Lite) 0x00400000 - 0x00593FFF (510D Lite)	NVM - APPL	Y	NVM for Cortex-M55/System Software
	0x005FC000 - 0x005FFFFF (510 Lite) 0x005B8000 - 0x005FFFFF (510B Lite) 0x00594000 - 0x005FFFFF (510D Lite)	NVM - M4[1]	Y	NVM for Cortex-M4 Firmware (510B Lite has BLE-only code; 510D Lite has Bluetooth Dual Mode: BR/EDR+ BLE)
	0x00600000 - 0x01FFFFF	Reserved	X	Reserved
	0x02000000 - 0x0201FFFF	Boot Loader ROM	Y	Boot Loader ROM (128 kB)
	0x02020000 - 0x1FFFFFFF	Reserved	X	Reserved
SRAM	0x20000000 - 0x2003FFFF	DTCM	Y	Instruction/Data TCM (256 kB)
	0x20040000 - 0x2007FFFF	Reserved	X	Reserved
	0x20080000 - 0x2023FFFF	System SRAM	Y	System SRAM (1.75 MB)
	0x20240000 - 0x2FFFFFFF	Reserved	X	Reserved
	0x30000000 - 0x3003FFFF	DTCM	Y	Instruction/Data TCM (256 kB) [Aliased to 0x20000000 - accessible only from Secure SW when TrustZone is enabled]
	0x30040000 - 0x3FFFFFFF	Reserved	X	Reserved
Peripheral	0x40000000 - 0x4FFFFFFF	Peripheral	N	See Peripheral Memory Map
	0x50000000 - 0x5FFFFFFF	Reserved	X	Reserved

Table 4: Cortex-M55 CPU Memory Map

Type	Address Range	Name	Executable	Description
External RAM	0x60000000 - 0x6FFFFFFF	MSPI0	Y	External Memory (256 MB)
	0x70000000 - 0x7FFFFFFF	Reserved	X	Reserved
	0x80000000 - 0x83FFFFFF	MSPI1	Y	External Memory (64 MB)
	0x84000000 - 0x87FFFFFF	MSPI2	Y	External Memory (64 MB)
	0x88000000 - 0x9FFFFFFF	Reserved	X	Reserved
External Device	0xA0000000 - 0xDFFFFFFF	Reserved	X	Reserved
Private Peripheral Bus	0xE0000000 - 0xE00FFFFF	PPB	N	NVIC, System timers, System Control Block, MPU, TPIU, ETB, EWIC (1 MB)
Vendor_ SYS	0xE0100000 - 0xFFFFFFFF	Reserved	X	Reserved

1. Factory-installed Cortex-M4 firmware reduces the amount of available NVM which varies for each series derivative. The NVM address range used in each derivative is as stated.

Peripheral devices within the memory map are allocated on 4 kB boundaries (mostly), allowing each device up to 1024 32-bit control and status registers. Peripherals will return undefined read data when an attempt to access a register which does not exist occurs. Peripherals will always accept any write data sent to their registers without attempting to return an error response. Specifically, a write to a read-only register would just become a don’t-care write.

Table 5 shows the memory map for the peripheral devices. The CPU has access to all peripheral devices. This table illustrates how SAU partitions are used to make certain peripheral regions secure when running with a TrustZone-secure partition enabled. OTP registers are separated from MRAM control to allow OTP registers to be secure via the SAU while the MRAM registers remain non-secure.

Table 5: Apollo510 Lite SoC Peripheral Memory Map

Address Range	Device Name
0x40000000 - 0x400003FF	Secure Reset/BoD Control (1 kB)
0x40000400 - 0x40003FFF	Reserved
0x40004000 - 0x400041FF	Secure Clock Generator (0.5 kB)
0x40004200 - 0x400047FF	Reserved
0x40004800 - 0x40004BFF	Secure RTC (1 kB)
0x40004C00 - 0x40004FFF	Reserved
0x40005000 - 0x40005FFF	Secure SSC (1 kB)
0x40006000 - 0x40007FFF	Reserved
0x40008000 - 0x40008FFF	Secure Timers (4 kB)
0x40009000 - 0x40009FFF	Secure MRAM and OTP CTRL (4 kB)
0x4000A000 - 0x4000A7FF	Reserved
0x4000A800 - 0x4000AFFF	Secure Miscellaneous Control (MCUCTRL) (2KB)
0x4000B000 - 0x4000BFFF	Reserved

Table 5: Apollo510 Lite SoC Peripheral Memory Map

Address Range	Device Name
0x4000C000 - 0x4000C3FF	Secure Power Control(1 kB)
0x4000C400 - 0x4000CFFF	Reserved
0x4000D000 - 0x4000D3FF	Secure Watchdog Timer (1 kB)
0x4000D400 - 0x4000E7FF	Reserved
0x4000E800 - 0x4000EFFF	SSC (1 kB)
0x4000F000 - 0x4000FFFF	Reserved
0x40010000 - 0x400103FF	Non-Secure RTC2 (1 kB)
0x40010400 - 0x40011BFF	Reserved
0x40011C00 - 0x40011FFF	Voltage Comparator (1 kB)
0x40012000 - 0x400127FF	Reserved
0x40012800 - 0x40012FFF	GPIO Control (2 kB)
0x40013000 - 0x400137FF	Reserved
0x40013800 - 0x40013FFF	Fast GPIO Control (1 kB)
0x40014000 - 0x40026FFF	Reserved
0x40027000 - 0x400273FF	Non-Secure Watchdog Timer 2 (1 kB)
0x40027400 - 0x4002FFFF	Reserved
0x40030000 - 0x40030FFF	Non-Secure Timers2 (4 kB)
0x40031000 - 0x40033FFF	Reserved
0x40034000 - 0x400343FF	BT IPC Mailbox
0x40034400 - 0x40034FFF	Reserved
0x40035000 - 0x400353FF	I^2C/SPI Subordinate: IOSFD0 (1 kB)
0x40035400 - 0x40035FFF	Reserved
0x40036000 - 0x400363FF	I^2C/SPI Subordinate: IOSFD1 (1 kB)
0x40036400 - 0x40037FFF	Reserved
0x40038000 - 0x400383FF	GPADC (1 kB)
0x40038400 - 0x40038FFF	Reserved
0x40039000 - 0x400393FF	UART0 (1 kB)
0x40039400 - 0x40039FFF	Reserved
0x4003A000 - 0x4003A3FF	UART1 (1 kB)
0x4003A400 - 0x4003FFFF	Reserved
0x40040000 - 0x400403FF	Simobuck SCM
0x40040400 - 0x4004FFFF	Reserved
0x40050000 - 0x40050FFF	I^2C/SPI Manager0 (4 kB)
0x40051000 - 0x40051FFF	I^2C/SPI Manager1 (4 kB)
0x40052000 - 0x40052FFF	I^2C/SPI Manager2 (4 kB)
0x40053000 - 0x40053FFF	I^2C/SPI Manager3 (4 kB)

Table 5: Apollo510 Lite SoC Peripheral Memory Map

Address Range	Device Name
0x40054000 - 0x40054FFF	I^2C/SPI Manager4 (4 kB)
0x40055000 - 0x40055FFF	I^2C/SPI Manager5 (4 kB)
0x40056000 - 0x40058FFF	Reserved
0x40059000 - 0x40059FFF	I3C Manager0 (4 kB)
0x4005A000 - 0x4005FFFF	Reserved
0x40060000 - 0x400603FF	MSPI Manager0 (1 kB)
0x40060400 - 0x40060FFF	Reserved
0x40061000 - 0x400613FF	MSPI Manager1 (1 kB)
0x40061400 - 0x40061FFF	Reserved
0x40062000 - 0x400623FF	MSPI Manager2 (1 kB)
0x40062400 - 0x4006FFFF	Reserved
0x40070000 - 0x400703FF	SDIO0 (1 kB)
0x40070400 - 0x40070FFF	Reserved
0x40071000 - 0x400713FF	SDIO1 (1 kB)
0x40071400 - 0x4008FFFF	Reserved
0x40090000 - 0x4009FFFF	Graphics Subsystem (64 kB)
0x400A0000 - 0x400A7FFF	Display Controller (32 kB)
0x400A8000 - 0x400AFFFF	Display PHY (32 kB)
0x400B0000 - 0x400B3FFF	USB (16 kB)
0x400B4000 - 0x400B7FFF	USB PHY (16 kB)
0x400B8000 - 0x400BFFFF	Reserved
0x400C0000 - 0x400C7FFF	Crypto (32 kB)
0x400C8000 - 0x40200FFF	Reserved
0x40201000 - 0x402013FF	PDM0 (1 kB)
0x40201400 - 0x40207FFF	Reserved
0x40208000 - 0x402083FF	I2S0 (1 kB)
0x40208400 - 0x41FFFFFF	Reserved
0x42000000 - 0x420007FF	NVM_INFO0 (2 kB)
0x42000800 - 0x42001FFF	Reserved
0x42002000 - 0x420037FF	NVM_INFO1 (6 kB)
0x42003800 - 0x42003FFF	Reserved
0x42004000 - 0x420040FF	OTP2_INFO0 (256 Bytes)
0x42004100 - 0x42005FFF	Reserved
0x42006000 - 0x42006AFF	OTP2_INFO1 (2816 Bytes)
0x42006B00 - 0x4FFEFFFF	Reserved
0x4FFF0000 - 0x4FFFFFFF	TB Debug (64 kB)

3.5 Static Random Access Memory (SRAM)

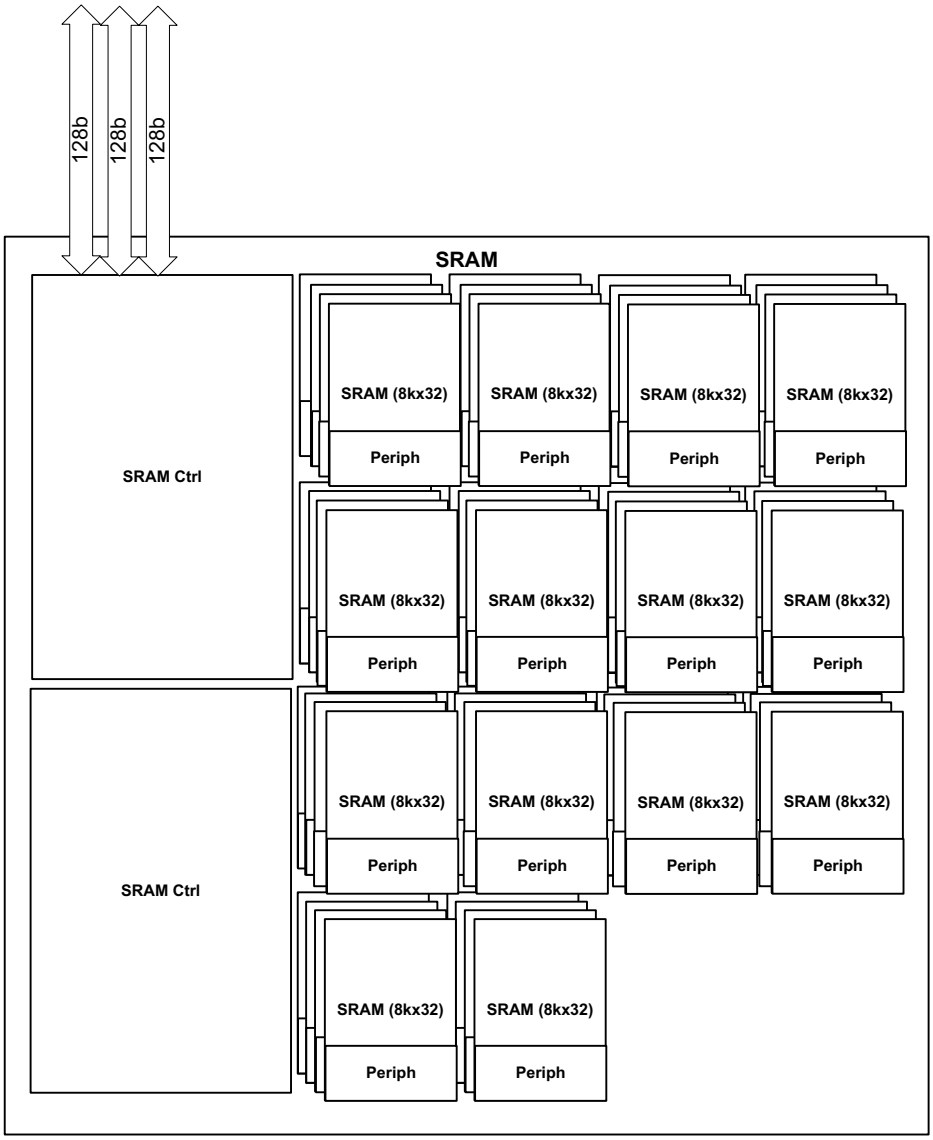

Figure 5. SRAM Block Diagram

3.5.1 Features

The Static Random Access Memory (SRAM) Controller supports features shown in Figure 5 and listed below.

- 1.75 MB total SRAM
- Fully synchronous design at 96 MHz (nominal)
- Three (3) 128-bit wide main AXI interfaces
- Internal arrays have 128 kB granularity. Each array can be concurrently accessed unless a physical conflict exists for the same 128 kB region.
- Supports concurrent operation to 3 independent 128 kB banks
- Partitioned into 2 power domains
- 1792 kB (standard) or 1024 kB, depending on product configuration

- Secure and non-secure partitioning is controlled via the CPU SAU
- Additional write/read protection bits supported for non-CPU access control (16 kB chunk size)

Please refer to the MCUCTRL registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

3.5.2 Functional Overview

The Apollo510 Lite SoC SRAM module provides up to 1.75 MB of shared internal SRAM for the system. It has three primary 128-bit AXI system interfaces and accommodates up to three simultaneous SRAM operations per cycle as long as the RAM bank doesn't overlap. Below are the port mappings:

- Port 0: Cortex-M55
- Port 1: DMA, Display Controller
- Port 2: Radio, GPU

3.6 OTP

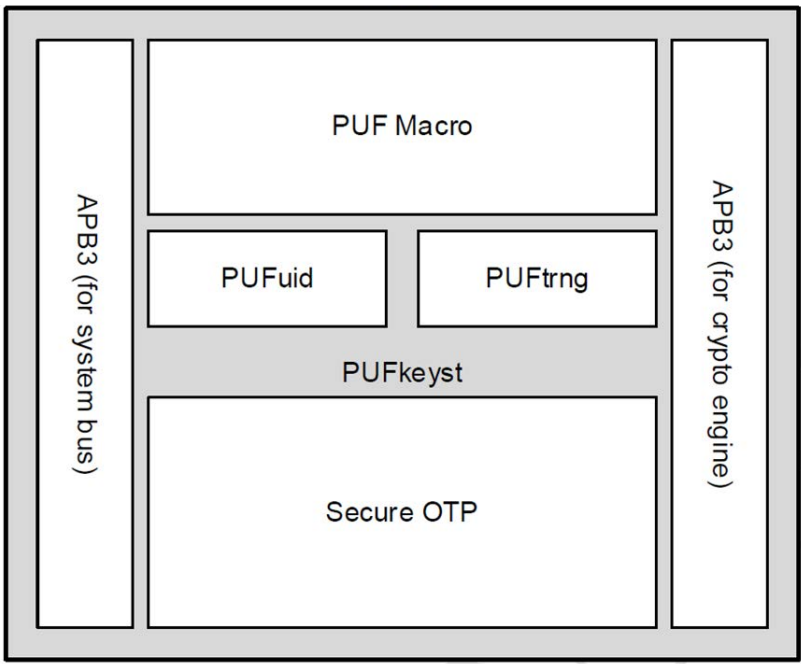

Figure 6. OTP Block Diagram

3.6.1 Features

The One-Time Programmable (OTP) and Physically Unclonable Function (PUF) include features[1] shown in Figure 6 and listed below.

- OTP anti-fuses
- PUFuid on NeoPUF: 2 kbits on-chip Identification
- PUFtrng: PUF-based True Random Number Generator
  - Conditioning & Entropy Health Test

3.6.2 Functional Overview

The OTP block on the Apollo510 Lite SoC includes multiple regions of OTP anti-fuse bits, anti-tampering support, read/write locking and dedicated interfaces for system and crypto access. The OTP anti-fuses are divided into the following three regions:

- INFO0: 256 bytes (2048 bits)
- INFO1: 1.375 kB (11 kbits)
- INFOC: 1024 bytes (8 kbits)

3.6.2.1 PUF Features/Functionality

PUF features[2] on the Apollo510 Lite SoC are described below.

- **NeoPUF**® - A weak PUF defined as a PUF with limited CRPs (challenge-response-pairs).

1. Some of the features are reserved for Ambiq use.
2. Certain functions have been protected and are only accessible to secure software if a secure execution environment (SEE) is instantiated.

  - Able to be used for generating true random bits which can act as a silicon fingerprint.
  - Has the near ideal PUF characteristics of 50% HW (Hamming-Weight), 50% Inter-HD (Hamming-Distance), 0% Intra-ID HD and 0ppm BER (Bit-Error-Rate).
  - Passes the NIST SP800-22 and NIST SP80090B IID statistical analysis test suites.
- **PUFuid®**
  - Offers 1 kilobit unique keys, which are derived from NeoPUF and programmed into PUF array in OTP by Ambiq. These keys can be used as a source for a unique ID, root key or entropy source, which is different for each chip.
- **PUFtrng®**
  - True random number generator with a PUF-based refinement engine.
  - Leverages 1 kilobits of PUF data for initial seeding.

3.6.2.1.1 PUF System Side Function Descriptions

System side function descriptions are as follows. PUF addresses listed are offsets from a base address of 0x40014800.

- **Get Random Number Output (0x02A0)**
  - Provides high-quality random number bits (32 bits each time) for security usage.
  - Open to all security levels unless memory range is mapped Secure.
- **Read UID (0x0300 - 0x037C)**
  - Reads from a 1 kilobit PUF Array which contains all the random data that is used for UIDs and the entropy source for the TRNG.
  - 32 UID locations ranging from 0x0300 to 0x037C.
  - Read the UID from PUF cell.
  - These registers are labeled puf_000 - puf_031.
  - Each PUF location provides 32 bits static entropy which can act as a silicon fingerprint for the various security applications of identification, authentication, and local data protection.
  - Only accessible to the Secure domain, if SEE is instantiated.

3.7 Additional Information

Please refer to the MCUCTRL and OTP registers of the Apollo510 Lite Series SoCs register set. The register set is delivered as part of the AmbiqSuite SDK.

4. System Power Management

System power management on the Apollo510 Lite Series SoCs is handled through a combination of hardware and software. The hardware handles the interface and control sequencing between the regulators and the individual power domains within the SoC. The software initiates transitions through power states by processor instructions and system level power control commands.

4.1 Functional Overview

The Power Management system is composed of a central power management controller and various power management units (PMUs) for each primary subsystem. The primary PMUs are as follows:

- CPU PMU: responsible for power sequencing for the CPU subsystem
- IO/Peripheral PMU: responsible for power sequencing at each I/O subsystem
- Memory PMU: responsible for power sequencing each memory subsystem/power bank

4.1.1 CPU Power Management Unit

When moving from Active Mode to Deep Sleep Mode, the CPU PMU manages the state-retention capability of the registers within the Cortex-M55 core and controls the interface to the voltage regulators as needed to support the various operating modes of the CPU. Once in the Deep Sleep Mode, the CPU PMU, in conjunction with the Wake-Up Interrupt Controller, waits for a wakeup event. When the event is observed, the CPU PMU begins the power restoration process by re-enabling the on-chip voltage regulators and restoring the CPU register state. The Cortex-M55 is then returned to active mode.

The CPU-PMU enables support for the following Arm Cortex-M55 defined power modes:

- OFF
- Deep Sleep
- Sleep
- Active
  - Low Power / High Efficiency: 96 MHz (LP)
  - High Performance: 192 MHz and 250 MHz
    - 192 MHz supported via HFRC oscillator clock (HP1)
    - 250 MHz supported via PLL (HP2) (Note: If concurrent with audio, the PLL frequency is limited to less than 250 MHz, depending on the audio use-case.)

4.1.2 IO/Peripheral Power Management Unit

The IO/Peripheral PMUs manage power state for I/O subsystems. Each I/O subsystem will support the following power modes. Note that each I/O subsystem may have a different implementation that defines each specific power state (i.e., what "Active" means). This is implementation-specific to each I/O controller. Also, not all power modes may be supported by each IO/Peripheral PMU (typical configuration may support only OFF and Active LP).

- OFF
- Sleep/Idle: device is enabled but no active transactions
- Active

4.1.3 Memory Power Management Unit

The Memory PMUs manage power state for the various memory subsystems. Each memory subsystem will support the following power modes.

- OFF (no memory retained for volatile RAM, power down mode for non-volatile memory)
- Retention (corresponding memory is held at retention level, all memory contents are maintained)
- Sleep/Idle (device is enabled but no active transactions)

- Active

Note that the primary power state for all memory in the SoC is dependent on the CPU power state. Once CPU goes into Deep Sleep mode, all memories can enter into retention or OFF mode (depending on the software configuration). When in this mode, DMA transactions or accesses from other peripherals (such as Graphics) are on-demand. On access, the PMU ensures the target memory is powered up into Active mode before servicing the transaction.

4.2 Power Management Controller

The power management controller provides control functions for each supply regulator as well as the primary power gates under digital logic control. The power management controller receives input from all PMUs indicating requested power levels and also controls from software (via power management control registers). A power management mapping configuration is also provided (sourced from trims shadowed to the power management controller) which dictates the functional operation at the regulator interface based on the input power requests. This mapping configuration allows the power management functionality to be programmatic enabling characterization, tuning and/or bug fixes.

Following are the supply regulator interfaces:

- SIMO Buck
- Core LDO
- Mem LDO

The central power controller is also responsible for controlling power gate enables for all digital power domains. The power gate enables are controlled based on the power level requests. When an “OFF” level is requested from the respective requester PMU or a software override is asserted to force a requester “OFF” or, for I/O requesters, when the corresponding I/O device enable is deasserted, the respective power gate enable is asserted to power off the domain. For all other power level requests, the power gate is disabled powering up the respective domain. It also controls the power muxes that source the various voltages to each of the corresponding power domains.

SSRAM and MRAM power domains are controlled based on the dependent requester domains. For MRAM, if CPU PMU requester is “OFF” *and* DMA requesters are “OFF” or “Sleep”, the MRAM power domain is powered OFF. For SSRAM, each SSRAM bank is powered OFF either based on the SKU memory configuration or if CPU requester is “OFF” *and* DMA requesters are “OFF” or “Sleep” and the SRAM is enabled to power off based on the power control MEMPWDINSLEEP configuration.

4.2.1 System Power States

At the SoC level, various power states are supported to enable key workloads and ensure maximum power efficiency. The system power states are defined in the following sub-sections. Mentioned in each of these system power state sections is the powering up and sleep mode retention of SRAM. SRAM consists of Shared SRAM (SSRAM) and Tightly Coupled Memory (TCM). The power-up and sleep mode retention settings for each of these memories is done via separate register settings whereby individual banks of SSRAM are selected to be powered on and their retention selected with the PWRCTRL_SSRAMPWREN_PWRENSSRAM field and the PWRCTRL_SSRAMRETCFG_SSRAMPWDSLP field, respectively. The power-up and sleep mode retention settings for TCM is done via the PWRCTRL_MEMPWREN_PWRENTCM field and the PWRCTRL_MEMRETCFG_TCMPWDSLP field, respectively. Note that in deep sleep mode, a portion, all or none of the enabled SSRAM/TCM can be selected for retention while in normal sleep mode whatever SSRAM/TCM is enabled is retained.

4.2.1.1 SYS Active (SACT)

The CPU is in one of the Active Modes and executing instructions. All respective memory and I/O devices are powered on and available as needed.

4.2.1.2 SYS Sleep Mode 0 (SS0)

SYS Sleep Mode 0 is a low power state for the SoC and can be entered if all processor cores are in sleep mode or deeper sleep state.

In this mode, the following conditions apply:

- All *enabled* SRAM memory (SSRAM and TCM) is retained (up to 2 MB).
- NVM memory is in standby.
- HFRC is on.
- Main core clock domain(s) is gated but peripheral clock domains can be on.

This state can be entered if a peripheral device (SPI/UART/I2C/MSPI, etc) is actively (or intermittently) transferring data and the time window is sufficient for processor(s) to enter Sleep Mode but is not long enough to go into a Deep Sleep Mode.

4.2.1.3 SYS Sleep Mode 1 (SS1)

SYS Sleep Mode 1 can be entered if all processor cores are in sleep mode or deeper sleep state, and all peripheral devices are idle and no peripheral device (SPI/UART/I^2C/MSPI, etc) is actively transferring data. However, communication may occur within a short time window which prevents the processor(s) from entering Deep Sleep Mode (and subsequently the system from entering a lower power state).

This state is also referred to as “Active Idle” whereby all power domains can be powered on but all clocks are gated. This state is a good power baseline for the system as it represents the active mode DC power level. Typically, the power in this state is dominated by leakage and always-on functional blocks.

In this mode, the following conditions apply:

- All *enabled* SRAM memory (SSRAM and TCM) is retained (up to 2 MB).
- NVM memory is in standby.
- HFRC is on.
- All functional clocks are gated.

4.2.1.4 SYS Deep Sleep Modes

There are 5 levels of SYS Deep Sleep Mode as described in the sub-sections below. Each of the five modes represents a deeper level of sleep and a proportionate reduction in power draw.

In Deep Sleep Mode 0-3, SRAM (SSRAM and TCM) can have a configurable amount of memory in retention depending on the software/system functional and latency requirements. SSRAM retention options, which do not include available selections for size of TCM retention (0, 128 kB, 256 kB depending on amount powered up), are the following:

- 1792 kB
- 1024 kB
- 768 kB
- 0 kB

The Instruction/Data TCM retention options in these modes are (1) all enabled TCM is retained, and (2) no TCM is retained.

4.2.1.4.1 SYS Deep Sleep Mode 0 (SDS0)

SYS Deep Sleep Mode 0 is a deep low power state for the SoC. This state can be entered if a peripheral device (SPI, UART, I^2C, MSPI, etc.) is actively or intermittently transferring data but the window of acquisition is long enough to allow the processor(s) to go into a deeper low power state.

In this mode, the following conditions apply:

- All processors are in Deep Sleep mode and/or are powered OFF.
- Configurable amount of SRAM (SSRAM and TCM) is in retention (capacity controlled by software).
- Cache memory is in retention.
- NVM memory is in power down.
- HFRC can be on depending on the state of the peripherals needing the HFRC clock.
- Main processor power domains are off but peripheral power domains can be on.

4.2.1.4.2 SYS Deep Sleep Mode 1 (SDS1)

SYS Deep Sleep Mode 1 is another deep low power state for the SoC. This state can be entered if the latency to warm up the cache can be tolerated. This could be an extended wait for a peripheral communication event.

In this mode, the following conditions apply:

- All processors are in Deep Sleep mode or are powered OFF.
- Configurable amount of SRAM (SSRAM and TCM) is in retention (capacity controlled by software).
- Cache memory is powered off (no retention).
- NVM memory is in power down.
- HFRC can be on depending on the state of the peripherals needing the HFRC clock.
- Main processor power domains are off but peripheral power domains can be on.

4.2.1.4.3 SYS Deep Sleep Mode 2 (SDS2)

SYS Deep Sleep Mode 2 is the minimum power state that the processor(s) can resume normal operation. This state can be entered when all activity has suspended for a duration of time sufficient to sustain the longer exit latencies to resume. This could be a state where periodic data samples are taken and the data is locally processed/accumulated/transferred at long time intervals. This state can only be entered (vs SDS1) if the peripheral devices are either not enabled/active or if the application can afford to save/restore the state of the controller(s) on entry/exit of this mode.

In this mode, the following conditions apply:

- All processors are in Deep Sleep or are powered OFF.
- Minimal SRAM (SSRAM and TCM) memory is retained as needed for software to resume.
- Cache memory can be powered off (or kept in retention).
- NVM memory is in power down.
- HFRC is off.
- XTAL can be on depending on the configuration of timers (either XTAL or LFRC is on).
- All internal switched power domains are off/gated.
- Processor logic state is retained.

4.2.1.4.4 SYS Deep Sleep Mode 3 (SDS3)

SYS Deep Sleep Mode 3 is a new "deeper sleep" state where minimal SSRAM and TCM memory is retained as needed for software to resume (note that SRAM can have configurable amount of instances in retention depending on the software/system functional and latency requirements). In this mode, the following conditions apply:

- All processors are in deep sleep or are powered OFF.
- Minimal SRAM (SSRAM and TCM) memory is retained as needed for software to resume.
- Cache can be powered off or kept in retention.
- HFRC is off.
- XTAL can be ON or OFF (either XTAL or LFRC is on).
- NVM memory is power down.
- All internal switched power domains are off/gated.
- Processor logic state is retained.

- All but 16 GPIO enter a power down state (core supply is power gated and I/O side state is determined by a set of GPIO isolation control signals).

This state has longer latency to resume but is the deepest low power state of the SoC with function retention mode.

4.2.1.4.5 SYS Deep Sleep Mode 4 (SDS4)

SYS Deep Sleep Mode 4 is a deep sleep power state that can be entered on long periods of inactivity.

In this mode, the following conditions apply:

- All processors are in Deep Sleep or are powered OFF.
- No memory is in retention, all memory is powered down.
- LFRC is on (HFRC and XTAL are off)
- All internal switched power domains are off/gated.
- Processor logic state is retained.
- Single timer is running.

4.2.1.5 SYS OFF Mode (SOFF)

In SYS OFF Mode, SoC is completely powered down with no power supplied. This mode is controlled external to the SoC by removing power to the device.

- Processors are in shutdown mode with no state retention.
- Only NVM memory is retained.

4.3 Program Control of Power Management

The transition between power modes is largely directed by software and the workload/task requirements.

4.3.1 Guidance for HP mode usage

There are 2 HP modes in Apollo510 Lite SoC - HP1 and HP2. HP1 runs at 192 MHz and HP2 at 250 MHz. HP1 sources its clock from the HFRC and, as such, is lower power but also lower deepsleep exit latency (<15 µs) as compared to HP2. HP2 sources its clock from the system PLL. As such, it is slightly higher power than HP1 and has a much longer exit latency from deepsleep (60-70 µs). There is a setting that allows deepsleep exit to HP1 and then to HP2 once the PLL locks (PWRCTRL_MCUPERFREQ:WAITFORHP2). Users must decide which setting to use, given their application requirements.

Since HP2 mode requires use of the system PLL, there are some additional considerations that should be taken into account when setting up. By default and for lowest power, it is recommended to use HFRC/4 (MCU_CTRL_PLLCTL0:FREFSEL = HFRCDIV4) as the reference clock to the system PLL. This assumes there are no active peripherals requiring high fidelity clocking (such as radio, HiFi audio or USB HS). Utilizing the WAITFORHP2 setting allows for maximum performance and lowest exit latency.

In the case where the radio is active (and high frequency XTAL is already active) or a high fidelity peripheral is configured/active (requiring the PLL and high frequency XTAL as the reference clock), the PLL is already enabled and configured to source from the high frequency XTAL. So, there is no additional penalty due to HP2.

Since the PLL requires time to ramp/lock, it is recommended that software initialize the PLL in advance of needing it. Note that hardware will ensure the PLL is enabled/brought up before acknowledging an HP2 entry request. Hardware will also sequence the PLL off/on for a deepsleep entry/exit accordingly. Again, to accelerate entry into HP2, it is recommended that software support a pre-config function call to configure and enable the PLL before the call to enter HP2. Note that this step will add power while the PLL is enabled but will reduce the latency to enter HP2 if this is required by the application.

4.3.2 CPU

Transitioning to different power modes is initiated through a couple methods depending on the software intent and performance/power/latency requirements. The different mode transitions are described in the following table.

Table 6: Transitioning among Power Modes

	Deep Sleep	Sleep	Active - LP	Active - HP
Sleep/ Deep Sleep	X	X	WAKE+LP	WAKE+HP
Active - LP	WFI (DS)	WFI (S)	X	HP
Active - HP	WFI (DS)	WFI (S)	LP	X

- WFI (DS): Issue WFI instruction Deep Sleep
- WFI (S): Issue WFI instruction Sleep
- LP: Write to CLKGEN_PERFREQ register indicating “LP”. Check CLKGEN_PERFSTAT to check if mode switch completed and if performance mode is available. Continue execution.
- HP: Write to CLKGEN_PERFREQ register indicating “HP”. Check CLKGEN_PERFSTAT to check if mode switch completed and if performance mode is available. Continue execution.

CPU active state transitions are controlled via the PWRCTRL_MCUPERFREQ register. Software requests the appropriate performance mode (LP or HP mode) by writing to the MCUPERFREQ field as appropriate. Software must check that it received an acknowledge of the performance mode request (by checking the MCUPERFACK and MCUPERFSTATUS fields. It is possible that the PMU will not honor a performance mode change request (i.e. in the case where max power condition might be exceeded). Once acknowledged, the CPU should be operating in the corresponding performance mode until software switches to a different mode.

4.3.3 I/O

The I/O power modes are determined by how the I/O controller is configured. For example:

- OFF: Controller power domain is OFF, “device enable” bit not set in power controller. This transition can also be made by the I/O PMU if auto-power-off is supported.
- Sleep: Controller is “device enabled” but the controller interface has not been enabled/activated (AKA IDLE). This transition can also be made by the I/O PMU if auto-power-on is supported.
- LP: This needs to be determined based on the operating mode of the controller. This typically will be for high performance interfaces (such as MSPI).

4.3.4 Memory

The memory power modes are determined by PWRCTRL register configuration and the relative state of the various mains in the SoC. The primary state of all memories is dictated by the CPU. Once the CPU goes into Deep Sleep mode, all memories can go into retention or power down mode. If any outstanding transaction exists for a given memory target, the power controller will keep that respective memory device powered in Active mode or will wake the memory from retention or power down mode. Once Active, the outstanding transaction can be completed. There are hysteresis counters to keep memories powered up for longer periods of time to avoid thrashing.

The memory is configured by PWRCTRL_MEMPWREN and PWRCTRL_MEMRETCFG (for MRAM, CPU TCM and cache memories) as well as PWRCTRL_SSRAMPWREN and PWRCTRL_SSRAMRETCFG (for Shared SRAM memories) registers. If a memory is not enabled, the retention configuration is a don't care. Only if enabled, the retention configuration applies and will be enforced whenever the respective memories can enter lower power states.

4.4 Additional Information

Please refer to the PWRCTRL registers of the Apollo510 Lite Series SoCs register set. The register set is delivered as part of the AmbiqSuite SDK.

5. Security

5.1 Apollo510 Lite SoCFeatures

The Apollo510 Lite SoC provides secure boot and security functions leveraging Ambiq's SecureSPOT™ technology, and additionally supports the Arm Platform Security Architecture (PSA) and is TrustZone® compliant.

Key security features include:

- Physically Unclonable Function (PUF)
- Tamper resistive fuses and key storage bank
- Secure Boot
- Secure Over-the-Air (OTA) Updates
- Secure Wired Updates
- Secure Key Storage
- Key revocation
- Secure debug
- Secure lifecycle management
- Crypto Subsystem (See "Crypto Subsystem" on page 53 for features and details.)

Please refer to the Security and Crypto registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

5.2 Functional Overview

Apollo510 Lite SoC adheres to Arm Platform Security Architecture (PSA). This establishes a secure processing environment that isolates security critical functionality and data from application software. The basis of the secure processing environment is a secure boot. This leverages the immutable Root-of-Trust (RoT) based on a set of hardware primitives which ensure trusted boot of the device. Maintaining the chain of trust is critical. The Apollo510 Lite SoC provides robust security services to support Over-the-Air (OTA) updates, wired updates and secure debug sessions.

Table 7: Security Domain Partitioning

Mode	Nonsecure	Secure	
		OEM Accessible	Ambiq Private Domain (APD)
Normal (non-privileged)		User Threads, Normal Applications, Normal Middleware	
Privileged		RTOS, Drivers, Privileged Threads, HAL, Privileged Middleware	BootRom, Helper Functions, Ambiq-Private Keys, Trims

The Ambiq Private Domain employs a variety of mechanisms to isolate the APD resources – see Security Locks below.

5.3 Physically Unclonable Function (PUF)

The Apollo510 Lite SoC incorporates a PUF that can be utilized by software and is used internally to secure the OTP memory, providing enhanced protection of assets. See "OTP" on page 40 for more information about PUF features.

5.4 Secure Boot

The Secure Boot feature on the Apollo510 Lite SoC provides a secure foundation for customer firmware/ services. The secure boot loader provides authentication, decryption and integrity validation for all firmware upon installation and boot/reset. Secure boot loader provides firmware recovery and OTA update support.

Secure Boot policy can be used to direct the secure boot loader based on the customer security requirements.

A high level flow diagram of the Secure Boot process is illustrated below in Figure 7. See the “Apollo5 Security Guide” for more details.

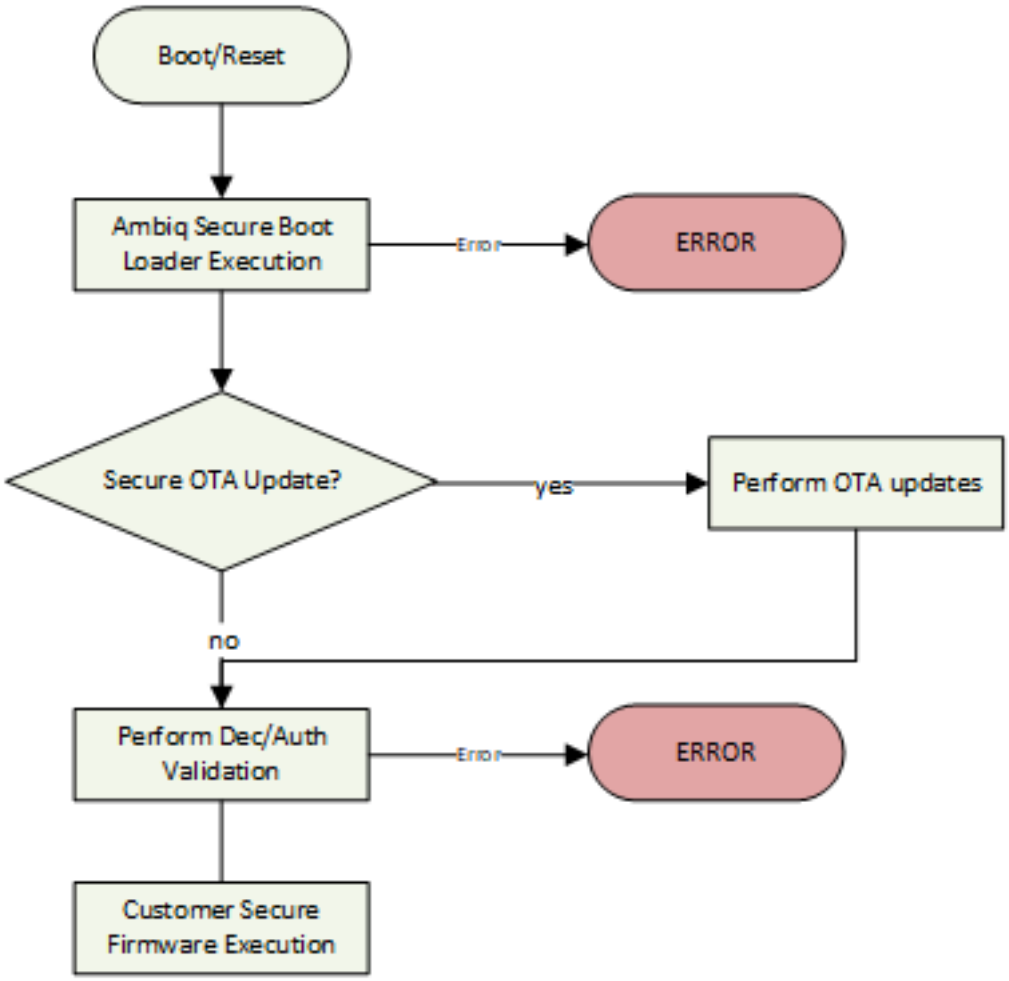

Figure 7. Secure Boot Process Flow Diagram

5.5 Secure OTA

The Apollo510 Lite SoC supports secure OTA leveraging the Ambiq secure boot loader. Customers can update any firmware component securely as directed via the security policy configuration. The basic Secure OTA flow is shown in Figure 8.

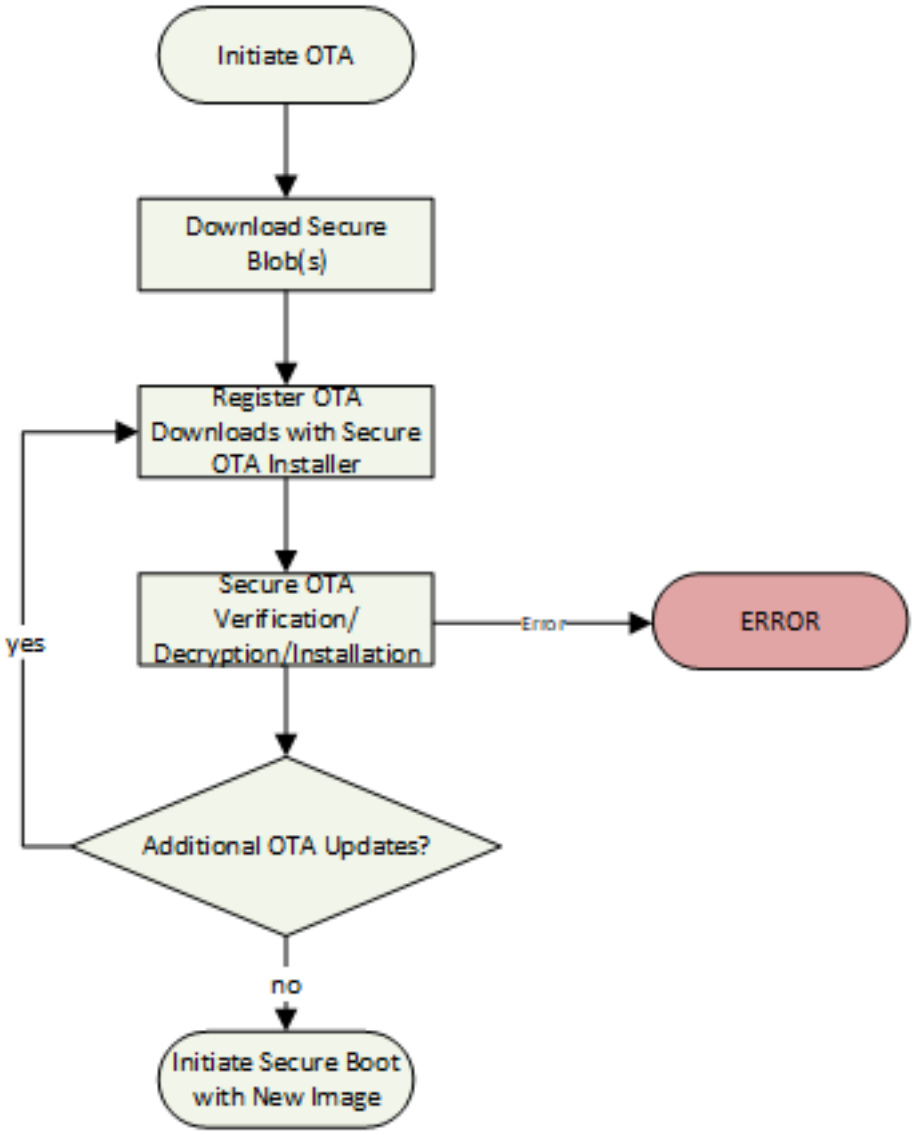

Figure 8. Secure OTA Flow Diagram

5.6 Secure Key Storage

Key material is managed by hardware and exposed to software via security APIs. The keys are stored securely in OTP memory and are never directly accessible to software. Certain key material is used/ accessible only during certain lifecycle state of the device. These are mainly used for provisioning of the device.

5.6.1 Software Keys

Additionally, there are “Software Keys” available to use in OTP (INFOC) that can be provisioned by OEM. These keys can be configured to be accessible only to privileged software (e.g., bootloader).

5.7 Secure Lifecycle States

The Apollo510 Lite SoC supports the following lifecycle states:

- Chip Manufacturer (CM)
- Device Manufacturer (DM)
- Secure
- RMA

The lifecycles are managed by hardware and OTP.

5.8 Secure Debug

The debug sub-system has been enhanced in the Apollo510 Lite SoC to provide separate capabilities for secure and nonsecure debug. If only nonsecure debug is enabled, then no secure resources may be accessed, and no secure code may be stepped into, debugged, or traced.

5.9 Crypto Subsystem

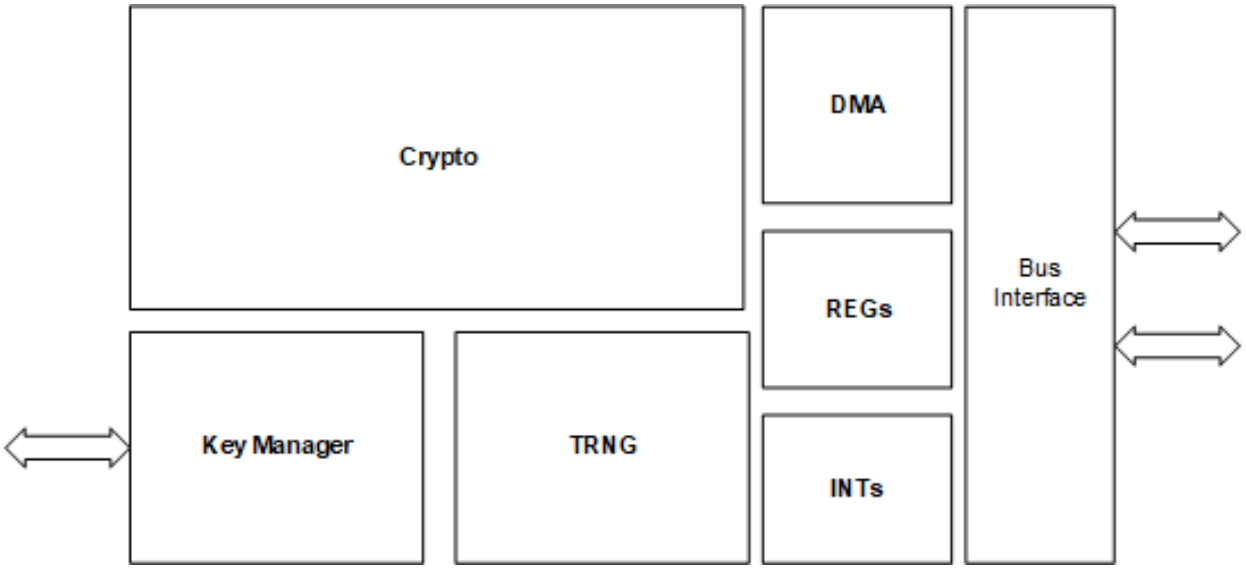

Figure 9. Crypto Subsystem Block Diagram

The Apollo510 Lite SoC's Crypto Subsystem provides the cryptographic acceleration and isolation required to support the Apollo5 family security model. These services are managed by software to support private and public-side cryptographic functions, and includes features shown in Figure 9 and listed below.

- Cryptographic acceleration for the protection of data-in-transit and data-at-rest.
- Protection of various assets belonging to the chip manufacturer (ICV) or device manufacturer (OEM), service operators providing services over the target device and the device. These asset protection features include:
  - Image verification at boot/during runtime
  - Authenticated debug
  - Random number generation
  - Security lifecycle state management
  - Asset Provisioning

The following standard specifications are supported:

- FIPS Publication 186-4: Digital Signature Standard (DSS), July 2013, compliant with sections 5.1, 6.2, 6.3, 6.4, B.1.2, B.2.2, B.3.6, B.4.2, C.3.1, C.3.3, C.3.5, C.9, and D.1.2.
- FIPS Publication 197: Advanced Encryption Standard, support only 128-bit and 256-bit keys.
- NIST SP 800-38A: Recommendation for Block Cipher Modes of Operation: Methods and Techniques, compliant with sections 6.1, 6.2, 6.4, and 6.5.
- NIST SP 800-38B: Recommendation for Block Cipher Modes of Operation: the CMAC Mode for Authentication
- NIST SP 800-108: Recommendation for Key Derivation Using Pseudorandom Functions, compliant with section 5.1.
- Standards for Efficient Cryptography Group (SECG): SEC1 Elliptic Curve Cryptography, 2000, compliant with sections 2.1.1, 2.2.1, 3.1.1, 3.2, 3.3.1, 3.6.1, 4, and 6.1.

5.9.1 Crypto Acceleration

The CryptoCell-312 crypto accelerator is available to both the secure and the nonsecure domains. The following cryptographic features are supported:

- AES (128, 192, 256 bit)
  - ECB, CBC, CTR, OFB
  - CMAC, CBC-MAC, AES-CCM, AES_GCM
- AES Key Wrapping
- CRC32 with crypto acceleration
- External storage inline encryption/decryption with crypto acceleration
- Diffie-Hellman (1024, 2048, 3072 bit)
  - ANSI X9.42-2003: Public Key Cryptography for the Financial Services Industry: Agreement of Symmetric Keys Using Discrete Logarithm Cryptography.
  - Public-Key Cryptography Standards (PKCS) #3: Diffie-Hellman Key Agreement Standard.
- ECC Key Generation (NIST and 25519 curves)
- ECIES
- ECDSA
- ECDH
- SHA1/SHA224/SHA256
- HKDF
- KDF
  - NIST SP 800-108: Recommendation for Key Derivation Using Pseudorandom Functions
- RSA PKCS#1 (2048, 3072, 4096b)
  - Public-Key Cryptography Standards (PKCS) #1 v2.1: RSA Cryptography Specifications
  - Public-Key Cryptography Standards (PKCS) #1 v1.5: RSA Encryption
- RSA Key Generation
- True Random Number Generator (TRNG)
  - BSI AIS-31: Functionality Classes and Evaluation Methodology for True Random Number Generators.
  - NIST SP 800-90B: Recommendation for the Entropy Sources Used for Random Bit Generation.

See more detailed information at the CryptoCell-312 page of the Arm Developer site.

5.10 Additional Information

Please refer to the Security and Crypto registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

6. Radio Subsystem (RSS)

The Apollo510B Lite SoC and Apollo510D Lite SoC of the Apollo510 Lite Series include a Radio Subsystem (RSS) which functionally is a wireless controller that integrates a multi-protocol 2.4 GHz transceiver and dedicated Cortex-M4 processor with a reduced feature set. The RSS works in conjunction with the main Arm Cortex-M55 application processor in running a wireless host stack.

6.1 Features

The RSS supports features listed below.

- Arm Cortex-M4F Processor
  - Floating point unit (FPU)
  - 48 MHz / 96 MHz Operating Modes
  - Wake-up interrupt controller with 80 interrupts
- Memory
  - 8 kB 2-way Associative Instruction Cache
  - 64 kB (Arm M4) Tightly Coupled RAM
  - 32 kB Exchange RAM
  - Instruction access to System NVM
  - Data access to all system memories
  - MPU: 8 regions
- CM4 Power Management block
- Wireless Baseband
  - 12 MHz / 24 MHz Operating Modes
  - Bluetooth Classic® and Bluetooth Low Energy 5.4
  - Supports multi-protocol concurrency
  - Supports WLAN and mobile wireless coexistence
- RF Transceiver
  - Single-ended RF port
  - On-chip matching network with 50 ohm RF input
- Clock sources (to the application processor)
  - Crystal oscillator for 48 MHz XTAL (integral part of the RF transceiver)
- Clock sinks (from the application processor)
  - 96 MHz clock (HFRC)
  - 32.768 kHz clock (LF XTAL)

NOTE
The CM4-based Radio Subsystem is a “closed” system. Connection to the SWD/SWO is not supported or available.

6.2 Functional Overview

At the center of the Radio subsystem is a 32-bit Arm Cortex-M4 core (CM4) with the floating point option. This 3-stage pipeline implementation of the Arm v7-M architecture offers highly efficient processing in a very low power design. The Arm v7-M Debug Access Port (M DAP) enables debugging access via a Serial Wire Interface from outside of the MCU which allows access to all of the memory. The CM4 supports the DSP and Security ISA extensions enabling high efficiency compute with secure and non-secure processing support.

The CPU has data access to all system memories, and instruction access to the 2 MB of non-volatile memory. All of the memory is memory mapped and accessible to the CPU. All of the memory accesses are

qualified based on the memory protection attributes (enforced within the CM4) and the system memory protection attributes (enforced within the system memory controllers).

The Cortex-M4 processor supports the Arm v7-M Protected Memory System Architecture (PMSA) that provides programmable support for memory protection using a number of software controllable regions. Memory regions can be programmed to generate faults when accessed inappropriately by unprivileged software reducing the scope of incorrectly written application code. The architecture includes fault status registers to allow an exception handler to determine the source of the fault and to apply corrective action or notify the system.

Reference the "Arm Cortex-M4 Processor Technical Reference Manual" for more details.

6.3 Wireless Baseband

6.3.1 WLAN Coexistence

The Apollo510 Lite Series provides a BT PTA subordinate coexistence interface that supports the most common WLAN/PTA manager implementations listed below.

6.3.1.1 Supported WLAN PTA Managers

1-Wire PTA

In the typical 1-Wire PTA, the WLAN/PTA device asserts a GRANT signal when WLAN is not busy transmitting or receiving. When GRANT is asserted, the Bluetooth radio is allowed to transmit or receive. This mode does not allow the external radio to request the 2.4 GHz ISM and is not recommended.

2-Wire PTA

In 2-Wire, the REQUEST is added with the GRANT signal, allowing the Bluetooth radio to request the 2.4 GHz ISM band. The WLAN/PTA device internally controls the prioritization between Bluetooth and WLAN, and, on a conflict, the PTA can choose to either GRANT Bluetooth or WLAN.

3-Wire PTA

In 3-Wire, the PRIORITY signal is added, allowing the Bluetooth radio to signify that a high- or low-priority message is either being received or transmitted. The WLAN/PTA device compares this external priority request against the internal WLAN priority, which may be high/low or high/mid/low and can choose to either GRANT Bluetooth or WLAN.

PRIORITY can be implemented as static or directional (enhanced) priority.

- Static: PRIORITY is either high or low during REQUEST asserted for the transmit or receive operation.
- Directional: PRIORITY is either high or low for a typically 20 µs duration after REQUEST asserted, but switches to low during receive operation and high during transmit operation.

The Apollo510 Lite Series SoCs support both static and directional PRIORITY implementations. The user chooses one via register settings.

4-Wire PTA

In 4-Wire PTA, the FREQ signal is added, allowing the Apollo510 Lite Series to signify an “in-band” or “out-of-band” message is either being received or transmitted. The channel used by the WLAN interface needs to be shared with the Apollo510 Lite Series via registers settings to allow the Apollo510 Lite Series to

assert FREQ or not. It allows the two RF devices to receive simultaneously but never to send at the same time. Thus the 4-Wire only makes sense when the “combined” / “simultaneous RX access” mode is supported by the application platform.

6.3.1.2 BT PTA Subordinate Logic

Table 8 describes the logic necessary for the conversion of wireless baseband signals into BT PTA subordinate coexistence interface to WLAN PTA managers.

Table 8: Wireless Baseband Signal Conversion

WLAN PTA Manager Signal	BT PTA Subordinate Port Direction
WLAN_COEX_GRANT	Input
WLAN_COEX_REQ	Output
WLAN_COEX_PRIORITY	Output
WLAN_COEX_FREQ[1]	Output

1. Obtained as a result of comparing values on the wireless baseband radio out interface bits 26:20 (radio_out[26:20]) to the BT PTA Subordinate register, where the Cortex-M4 network core stores the information obtained from the main MCU about the WLAN channel (an offset from 2402 MHz).

Please note that all WLAN_COEX_[A-Z]+ ports share IO pads with other interfaces.

6.3.1.3 BT PTA Subordinate Registers

BT PTA subordinate contains the following user-programmable registers:

1. Programmed polarity for each WLAN_COEX_[A-Z]+ of WLAN PTA Manager signals, regardless of the direction.
2. WLAN channel storage register. This value is used for generating in-band/out-of-band state (FREQ signal).

6.3.2 Mobile Wireless System Coexistence

Wireless baseband supports the following MWS interfaces:

- Wireless Coexistence Interface 1 (WCI-1)
- Wireless Coexistence Interface 2 (WCI-2)

MWS interface selection is done via MWS interface configuration register(s) located in the wireless baseband wrapper.

The Apollo510 Lite Series SoCs’ WCI IO, ST_WCI_TXD and ST_WCI_RXD, are multiplexed with other interfaces.

Table 9 specifies wireless baseband connectivity to the Apollo510 Lite Series SoCs’ WCI IO.

Table 9: Wireless Baseband Connectivity to the Apollo510 Lite Series SoCs' WCI IO

Wireless baseband MWS port	WCI-1 Connectivity[1]	WCI-2 Connectivity
mws_wci_rxd (input)	IOMUX: ST_WCI_RXD (input)	IOMUX: ST_WCI_RXD (input), pull-up and pull-down disabled
mws_wci_txd (output)	IOMUX: ST_WCI_RXD pull-up control: 0: pull-up disabled 1: pull-up enabled	IOMUX: ST_WCI_TXD (output)
mws_wci_txd_pd (output)	IOMUX: ST_WCI_RXD pull-down control: 0: pull-down disabled 1: pull-down enabled	Not in use

1. The Apollo510 Lite Series SoCs have internal pull-up/pull-down resistors of values compliant with the Bluetooth Core Specification.

6.4 Arm Cortex-M4 Network Processor Architecture

6.4.1 Radio Subsystem Reset

Refer to "Reset Generator (RSTGEN)" on page 59 for details about different reset sources.

7. Reset Generator (RSTGEN)

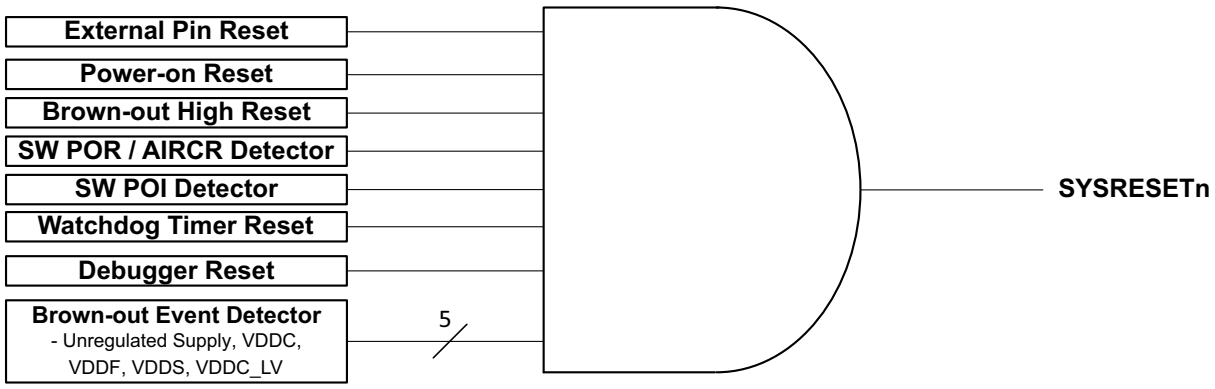

Figure 10. Reset Generator Module Block Diagram

7.1 Features

There are various resets that can be initiated in the Apollo510 Lite SoC. Depending on the level of reset, certain functions may get cleared or may persist values or executing across specific reset assertions. In all cases, the source of a reset is captured in RSTSTAT register.

The Reset Generator Module (RSTGEN) supports reset sources shown in Figure 10 and listed below.

- External reset pin (RSTn)
- Power-on event (POA)
- Brown-out event (BODL)
- Software requests
- Debugger request
- System request (AIRCR SYSRESETREQ from the Cortex-M55)
- Watchdog expiration

7.2 Functional Overview

The Reset Generator Module (RSTGEN) monitors a variety of reset signals and asserts the active low system reset (SYSRESETn) accordingly. A reset causes the entire system to be re-initialized, and the cause of the most recent reset is indicated by the STAT register.

There are four levels of reset on the Apollo510 Lite SoC:

- SYSRESETn System Software Reset
- Software POR Reset
- Software POI Reset
- Power-on Analog (POA) Reset

SYSRESETn is triggered by AIRCR.SYSRESETREQ, a Cortex-M55 warm reset.

Most resets trigger a POR reset, which is a shallow reset. This includes a Watchdog reset, a pin (RSTn) reset and a Cortex-M55 cold reset.

A POI reset is the deepest digital reset affecting hardware subsystems.

POA is the very deepest reset, digital and analog, and is only triggered by voltage going below POA voltage.

The effect of each of these reset levels on SoC modules and functionality is summarized in the following table and described in more detail in the following sections.

> NOTE
>
> There is a delay of 500 µs after a POR reset trigger before the reset actually occurs. During this delay the CPU continues to execute instructions.

Table 10: System Level Reset Summary Table (Reduced)

Action	IWIC Reset	MCU Warm Reset, Async Reset	TPIU Reset	Debug Reset	MCU Cold Reset, D-AHB/ EPPB Reset	PMU Reset[1], Power Control Reset	RTC/ STimer Reset
POA	x	x	x	x	x	x	x
POI, SW POI, Brownout	x	x	x	x	x	x	
Watchdog, Reset Pin, SW POR[2]	x	x	x	x	x		
SYSRESETREQ	x	x					
TPIU SW Disable, SW TPIU			x				
CDBGRSTREQ, SW DBG Reset			x	x			
SW IWIC Reset	x						

1. PMU is not fully reset, but the reset generator will send a request signal to the PMU so that it can sequence the WARM RESET. The signal is asserted one-half clock cycle earlier than the other resets to allow the PMU time to sequence the reset. Similarly, the PWRCTRL state machines are not reset, but the PWRCTRL register values are reset.
2. SW POR behaves exactly like POI except that the INIT state is retained. In particular, the debugger is reset by SW POR.

7.3 External Reset Pin

The active-low RSTn pin can be used to generate a reset using an off-chip component (e.g., a push-button). An internal pull-up resistor in the RSTn pad enables optional floating of the RSTn pin, and a debounce circuit ensures that bounce glitches on RSTn does not cause unintentional resets. The RSTn pin

is not maskable. An internal pull-down device will be active during a brownout event pulling the RSTn pin low. See Figure 11.

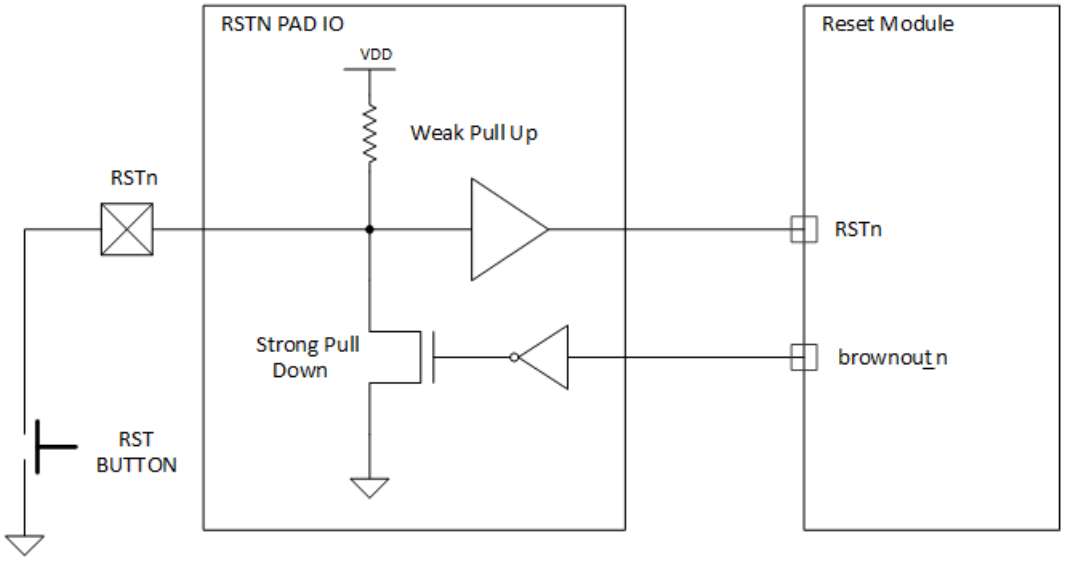

Figure 11. Block Diagram of Reset Pin Circuitry

7.4 Power-on Event

An integrated power-on detector monitors the supply voltage and keeps SYSRESETn asserted while VDD is below the rising power-on voltage, V_{POR+}. When VDD rises above V_{POR} at initial power on, the reset module will initialize the low power analog circuitry followed by deassertion of SYSRESETn, and normal operation proceeds. SYSRESETn is re-asserted as soon as VDD falls below the falling power-on voltage, V_{POR-}. The power-on reset signal, PORn, is not maskable.

7.5 Brown-out Events

Apollo510 Lite SoCAn integrated brown-out detector monitors the primary supply voltage and causes an automatic and non-configurable reset when the voltage has fallen below the low brownout threshold (BODL).

An additional integrated brown-out detector tracks the VDDRF supply voltage and triggers an interrupt if the voltage drops below the brownout threshold (trimmable from -100mV to -35mV).

In addition, there are individual brownout detector monitors integrated within the core/memory which cause separate/maskable reset assertions when the voltage falls below a critical level for the respective voltage rails - VDDC, VDDC_LV, VDDS or VDDF. In the event any of the supply voltages fall below its corresponding core/memory threshold if enabled, the reset module will initiate a system reset, enabling the RSTn pull-down and driving the reset pin low. The occurrence of a brownout reset will be reflected by the setting of the associated bit in the RSTGEN's INTSTAT Register after reset

In the event of a brownout detection, the following functionality is maintained until a power down detection occurs.

- All RTC registers retain state.
- RTC and STIMER counters continue operation from 32 kHz XTAL or from LFRC (if below BODL). If clock sources stop oscillating at very low voltage, the RTC and STIMER will continue to maintain state.
- Clock configuration registers retain state.

7.6 Software Reset

The SYSRESETn reset may be generated via software using the Application Interrupt and Reset Control Register (AIRCR) defined in the Cortex-M55. For additional information on the AIRCR, see the Arm document titled “Cortex-M55 Devices Generic User Guide.” The software reset request is non-maskable.

A second source for the identical software reset functionality is made available through the SWPOR register in the RSTGEN peripheral module. This reset causes a reset to all blocks except for registers in CLKGEN, RTC, STIMER and the power management unit. Most resets trigger a POR reset, which is a shallow reset. POR doesn't affect CLKGEN except that it sets the CPU clock to 96 MHz.

A third source of reset, which is the deepest digital reset affecting hardware subsystems, is made available through the SWPOI register. Writing the key value (0x1B) to this register triggers a Software POI reset, which causes:

- INFO space settings to be reloaded from Flash.
- a reset of all blocks except for registers in the RTC and the STIMER.
- the reloading from trim of the OSEL bit to the CLKGEN_OCTRL register, which selects either the LFRC or the XTAL to be used as the RTC clock source.
- reset of the CLKGEN features such as registers, CPU clock, and HFADJ - everything else is reset only by POA.

7.7 Watchdog Reset

The Watchdog Timer sub-module generates an interrupt if it has not been properly managed by software within a pre-defined time. The watchdog reset is maskable.

7.8 Additional Information

Please refer to the RSTGEN registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

8. Clock Generator (CLKGEN)

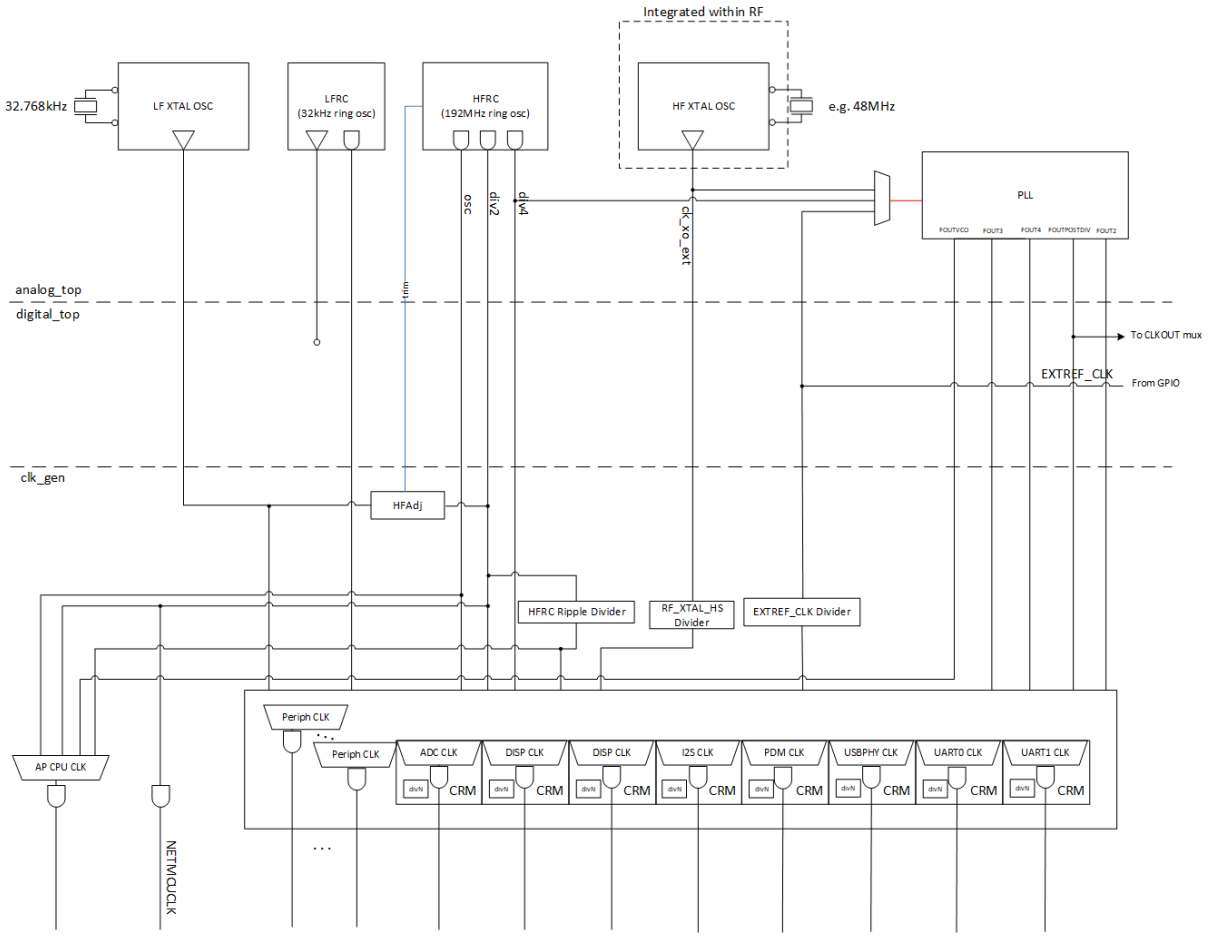

Figure 12. Block Diagram for Clock Generator Module

8.1 Features

The Apollo510 Lite SoCs clock generation subsystem is responsible for generating all of the primary and derived clocks in the SoC.

- Independent frequency scaling for various SoC subsystems
- Ultra low power, low frequency clock generation with XTAL calibration
- Programmable I/O clock dividers
- High precision audio clock generation
- High precision / low jitter PLL for high-fidelity audio and high-speed USB

NOTE
When enabling a module which automatically starts clocking with a default clock source, or when changing the clock source for any enabled module, there is a required 30 µs settling time for the selected clock.

8.2 Functional Overview

A high-level view of the Clock Generator Module, which supplies all clocks required by the Apollo510 Lite SoC, is shown in Figure 12. Note that the output clock frequencies from the clock sources are nominal values. Consult the Electrical Characteristics section for specified values.

8.2.1 Clock Generation Subsystem

The clock generation subsystem consists of the following sub-modules:

- Low-frequency crystal oscillator circuit (XTAL)
- High-frequency crystal oscillator circuit (RF-integrated)
- High-frequency RC oscillator (HFRC)
- Low-frequency RC oscillator (LFRC)
- High-frequency PLL circuits
- SoC clock generation logic
- Audio subsystem clock generation logic

8.2.1.1 Low-Frequency Crystal Oscillator (XTAL)

The high accuracy XTAL Oscillator is tuned to an external 32.768 kHz crystal, and has a nominal frequency of 32.768 kHz. It is used when frequency accuracy is critically important. To minimize power consumption, the XTAL is only enabled when an internal module is using it.

It should be noted that the XTAL oscillator is also optional if the requirements of the design can tolerate the internal LFRC/HFRC oscillator specifications.

External load capacitors are required to tune the XTAL oscillator circuit. Refer to “Clocks/Oscillators” on page 216 for more guidance and specifications.

NOTE

The XTAL is highly sensitive to external leakage on the XI pin. Therefore it is recommended to minimize the components on XI and to use extremely low leakage load capacitors.

The RTC clock source, either the LFRC Oscillator or the XTAL Oscillator, is selected via the CLKGEN_OCTRL_OSEL bit. If the XTAL Oscillator experiences a temporary failure and subsequently restarts, the Apollo510 Lite SoC will switch back to the XTAL Oscillator.

A 32 kHz reference clock is output from the XTAL circuit to several GPIO pins on all packages.

8.2.1.2 High-Frequency Crystal Oscillator

The high-frequency crystal from the RF subsystem (RF XTAL) is leveraged to provide a clean XTAL clock reference for the PLL, which can be configured as the clock source for audio peripherals, and used as a direct clock source to the USB subsystem. An alternate reference clock is supported via a GPIO input pin. This external clock source can also be used as a PLL reference (if needed to keep internal audio peripherals synchronous with an external codec/device clock) or directly as a clock source if needed as a supply to various peripheral devices. If not using USB high speed, the HFRC_div4 clock can be used as the USB clock source. Otherwise, if USB high speed is used, then RF XTAL must be used to clock the USB. In this case USB can be clocked by the RF XTAL directly (recommended) or by clocking USB via the PLL clocked by the RF XTAL.

8.2.1.3 Low-Frequency RC Oscillator (LFRC)

The low frequency RC block (LFRC) provides the low frequency clocks for timers and other logic within the SoC.

8.2.1.4 High Frequency RC Oscillator (HFRC)

The high-frequency RC oscillator (HFRC) provides all the primary clocks for the high-frequency digital processing blocks in the SoC except for audio, radio and HP mode clocks. These clocks are gated/ selected based on performance requirements. The digital clocks are isolated to avoid noise injection into the critical clocks for audio and radio communications. Additionally, the high-frequency digital clock is programmatically divided to generate the various I/O clocks in the system. All high-frequency clocks can be gated if not needed. The HFRC also supports a frequency-locked loop (FLL) circuit to ensure the HFRC oscillator locks to a specific frequency range to ensure high quality/low ppm output reference. The HFRC uses the 32 kHz XTAL as the reference clock for calibration.

8.2.1.5 System PLL

The system PLL is used to generate the high precision clocks needed for the USB reference clock and audio clocks. All PLL settings are controlled by software via MCUCTRL registers: PLLCTL0, PLLDIV0, PLLDIV1 and PLLSTAT.

MCLK output is provided from the PLL output to support external audio devices needing MCLK reference clock for synchronizing data transfer.

8.2.1.6 External Reference Clock Input

An external reference clock input, EXTREFCLK, can be used to provide an alternate reference clock source as needed to synchronize various clock generators within the SoC (such as the system PLL, DSI and/or USB PLL) to avoid interference or spur injection when in the Bluetooth enabled configurations.

8.2.2 Clocking Modules with the Clock/Reset Module (CRM)

This section describes what is needed to clock a module with the CRM. Modules supported by CRM are the following:

- I2S (MCLK / MCLKOUT / REFCLK)
- PDM
- ADC
- Display Controller
- Display PHY
- DSI DPHY PLL
- UART0/UART1
- USB

The procedure to set the clock for a domain/module using the CRM is as follows:

1. Software can reset a clock domain any time by clearing the clock domain’s RSTN bit in its PERIPH_CRM register. This will immediately reset the peripheral.
2. To ensure that the current and new clock sources are active, the CLKSEL field should be read before clearing the CLKEN bit.
3. Software should clear the CLKEN bit and poll for the CLKACTIVE bit to go low (clock disabled and not ready).
   - Software should then set the clock source (CLKSEL field) and the clock divider (CLKDIV field) in the module’s PERIPH_CRM register. CRM supports integer divide options for select modules with CRM. (CLKDIV is zero-based, i.e., 0 = DIV1, 1 = DIV2, etc.)
4. After setting the clock select and clock divider, software should set the CLKEN bit of the PERIPH_CRM register. No other clock or reset dependency is needed to change the clock.

Some sequence-related points to keep in mind are:

- For peripherals with multiple clock domains, there is one CRM per clock domain.

- An APB*CRM (* = module name) register controls the register clock domain of a peripheral. It is named APB*CRM because the register clock (PCLK) comes from the APBDMA block.The general rule is to set up the APB*CRM first followed by the functional clock's CRM.
  - The *RSTN field (bit 2 if it exists) resets the logic clocked by the clock output by the specific CRM.
  - The *CRMRSTN field (bit 3) resets the CRM logic (not its registers), as well as the logic clocked by the CRM's clock output.
- To shut a module down, its APB*CRM is shut down last.
- Hardware handles the dominant/subordinate relationship between PWRCTRL and CRM, when PWRCTRL controls clock/reset. In this case the sequence does not matter. if CRM is enabled but power is off, there is no clock downstream.
- When turning off the clock, software must wait for CLKACTIVE to be cleared.
- When turning on the clock, it depends on the peripheral whether polling for CLKACTIVE = 1 is needed.
- Some peripherals, which can be identified in the PERIPH_CRM register set, request its clock to be active dynamically based on its operation. For such clock domains, polling CLKACTIVE = 1 might cause a deadlock if the peripheral is turning off the clock itself.
- Generally, for APB*CRM, software needs to ensure that CLKACTIVE = 1 before accessing the registers of the peripheral as, without a clock, there could be an issue with the access.
- RSTN and CLKEN can be set and cleared in a single register write.

8.3 Clock Sources for the Apollo510 Lite SoC

Clock sources used within the SoC are as shown in Table 11. All clock sources except for the external reference clock (EXTREFCLK) can be gated.

Table 11: Requirements for Clock Sources

Clock Name	Frequency	Tolerance	Duty Cycle (% High/ Low)	Gateable	Additional Requirements / Comments
HFRC_48MHz	48 MHz	±5%	50/50	Yes	
HFRC_96MHz	96 MHz	±5%	50/50	Yes	Core clock
HFRC_192MHz	192 MHz	±5%	30/70	Yes	Burst or oscillator clock
LFRC_1kHz	900 Hz	±10%		Yes	
RF_XTAL_HS[1]	48 MHz	±20 ppm post calibration; ±40 ppm uncalibrated	50/50	Yes	
XT_32KHz[2]	32.768 kHz	±50 ppm[3]	50/50	Yes	
EXT_REFCLK	Variable depending on the external clock source			Yes	
PLLVCO	Typically 60 to 70 MHz, depending on application		50/50	Yes	
PLLPOSTDIV	Typically. 2 to 4 MHz, depending on applica-tion.				Supports various divide ratios
PLLFOUT2	div4 divide from FOUTPOSTDIV				
PLLFOUT3	div6 divide from FOUTPOSTDIV				
PLLFOUT4	div8 divide from FOUTPOSTDIV				
MCLK	24.576 MHz				Supports various divide ratios

1. See Clocks/Oscillator section of Electrical Characteristics for the specifications and range of frequencies supported by the high frequency XTAL.
2. See Clocks/Oscillator section of Electrical Characteristics for the specifications of the 32 kHz XTAL.
3. Depends on the accuracy of the external 32 kHz crystal. See Clocks/Oscillator section of Electrical Characteristics for crystal requirements.

Clocks used by the CPU, SRAM and NVM are as listed in Table 12.

Table 12: CPU, Memory and Storage Clocks

Block	Clock	LP		HP1		HP2		Additional Requirements / Comments
		Frequency	Source	Frequency	Source	Frequency	Source	
CPU	CLKIN	96 MHz	HFRC, HFRC_DIV4	192 MHz	HFRC Oscillator Clock	250 MHz	PLLVCO	HP2 requires PLL to be powered/configured/ enabled prior to switch to 250 MHz mode
	IWICCLK	96 MHz	HFRC	192 MHz	HFRC Oscillator Clock	250 MHz	PLLVCO	Synchronous with CLKIN, same frequency when in use. Gated during sleep. Can be ungated when CLKIN is gated. Must be ungated if CLKIN is ungated.
	PMUCLK	24 MHz	HFRC_DIV4	48 MHz	HFRC Oscillator Clock DIV4	62.5 MHz	PLL-VCO_DIV4	Asynchronous with CLKIN; sourced from the same clock trunk but divided by 4. Gated when not in use. Can be ungated when CLKIN is gated, but must track last CLKIN Source.
	STCLK	3 MHz	HFRC_DIV32					Asynchronous Clock; 1 MHz sufficient. Should be gated when CLKIN is gated, ungated when CLKIN in ungated.
	DBGCLK	See Debug section in Table 13						Synchronous with CLKIN, Gated when not in use. Can be ungated when CLKIN is gated, but must track last CLKIN source.
	TRACECLKIN	See Debug section in Table 13						Asynchronous, Gated. Arm recommends that this match the maximum frequency of the CPU clock.
	SWCLKTCK	See Debug section in Table 13						Input clock on SWJ DAP interface.
Shared SRAM/ Fabric	AXICLK	96 MHz	HFRC					
NVM	Bus Clock	96 MHz	HFRC					

Clock sources and divider options used by the modules and sub-systems on the SoC are as listed in Table 13.

Table 13: Module Clocks and Dividers

Module / Subsystem	Clock Node	Frequency	Source / Frequency Selections	Additional Requirements / Comments
USBPHY	utmi_refclk	12 MHz or 24 MHz	• EXT_REFCLK (12, 24, 48 or 96 MHz) • RF_XTAL_HS (48 MHz) • HFRC48 (48 MHz) • PLL FOUT2 (12 MHz or 24 MHz) • PLL FOUTPOSTDIV (12, 24, 48 or 96 MHz)	Supported CRM dividers: 1 - 8. PLLFOUT requires PLLVCO to be 240 MHz. Should be used in special cases where an external reference clock is required which is not a multiple of 12 MHz, i.e., 26 MHz TCXO.
	Bus Clock	96 MHz	• HFRC	
USB Controller	Bus Clock	96 MHz	• HFRC	
DSIPHY	Transmit Clock 12 MHz		• HFRC	Supported CRM dividers: 1 - 8.
DSIPHY	TxClkEsc (also serves as DPHY PLL reference clock)	Variable, (10 MHz - 20 MHz)	• EXT_REFCLK (up to 100 MHz) • RF_XTAL_HS (48 MHz) • HFRC/HFAdj div2 (48 MHz) • PLL FOUT2 (up to 25 MHz) • PLL FOUTPOSTDIV (up to 100 MHz)	Supported CRM dividers: 1 - 8.
	Bus Clock	96 MHz	• HFRC	
MSPI	MSPI0: IO_CLK	96, 125, 192 and 250 MHz	MSPI0 Sources: • 125, 250 MHz: PLLVCO • 192 MHz: HFRC Oscillator Clock • 96 MHz: HFRC	Each MSPI's I/O Clock source/divider selected by CLKGEN_MSPIIOCLKCTRL register. Each MSPI core clock can be divided by 1, 2, 3, 4, 6, 8, 12, 16, 24 or 32 by MSPI_DEVnCFG_CLKDIVn.
	MSPI1, MSPI2: IO_CLK	96, 125 and 192 MHz	MSPI1, MSPI2 Sources: • 125 MHz: PLLVCO • 192 MHz: HFRC Oscillator Clock • 96 MHz: HFRC	
	Bus Clock		• HFRC_96MHz	
SDIO0/1	Ref Clock	24, 48 and 96 MHz	• 24 MHz: HFRC_24MHz • 48 MHz: HFRC_48MHz • 96 MHz: HFRC_96MHz	Source synchronous. xin_clk is fixed to HFRC_96MHz in the SDK software. HFRC_48MHz and HFRC_24MHz are in the MCUCTRL_SDIOnCTRL registers as options.
	Bus Clock	96 MHz	• HFRC	
Crypto	Core Clock	96 MHz	• HFRC	
GFX	Core Clock	96 MHz	CLKGEN_CLKCTRL_GFXCORECLKSEL: • HFRC_96MHz	96 MHz is only option for GPU core clock.
	Bus Clock	96 MHz	• HFRC_96MHz	
Display Controller	Bus Clock	96 MHz	• HFRC_96MHz	
	Pixel Clock	Variable up to 200 MHz	• DPHY (TxByteClkHS, 96 MHz max) • HFRC oscillator clock (192 MHz) • PLL VCO (up to 250 MHz)	Supported CRM dividers: 1 - 16. DPHY (TxByteClkHS, 96 MHz max) is a primary clock source, HFRC or PLL is an alternative clock source for two-lane support.

Table 13: Module Clocks and Dividers

Module / Subsystem	Clock Node	Frequency	Source / Frequency Selections	Additional Requirements / Comments
Audio Subsystem	AUD_MCLK_OUT	Variable up to 100 MHz	• EXT_REFCLK (up to 100 MHz) • RF_XTAL_HS (48 MHz) • HFRC48 (48 MHz) • PLL FOUT4 (up to 12.5 MHz) • PLL FOUT3 (up to 16.6 MHz) • PLL FOUTPOSTDIV (up to 100 MHz)	Supported CRM dividers: 1 - 32.
	PDM I/O CLK	Variable 512 kHz - 3072 kHz	• PDM MCLK	.
	PDM MCLK	Variable up to 50 MHz	• EXT_REFCLK (up to 100 MHz) • RF_XTAL_HS (48 MHz) • HFRC48 (48 MHz) • PLL FOUT4 (up to 12.5 MHz) • PLL FOUTPOSTDIV (up to 100 MHz)	Supported CRM dividers: 1 - 128.
	PDM Bus Clock	96 MHz	• HFRC	
	I^2S I/O SCLK: 128-3027 kHz	512 kHz - 24576 kHz	• I^2S SCLK	
	I^2S MCLK	Variable 48 kHz - 50 MHz	• HFRC48 (48 MHz) • EXT_REFCLK (up to 100 MHz) • RF_XTAL_HS (48 MHz) • PLL FOUT4 (up to 12.5 MHz) • PLL FOUT3 (up to 16.6 MHz) • PLL FOUTPOSTDIV (up to 100 MHz)	Supported CRM dividers: 1 - 128. PLL output frequency is selected by MCUCTRL_PLLMUXCTRL register: • PLLFOUT3 is FOUTPOSTDIV divided by 6, or nominal 8 MHz based on 48 MHz PLL clock ref. • PLLFOUT4 is FOUTPOSTDIV divided by 8, or nominal 6 MHz based on 48 MHz PLL clock ref. All others selected by I2S_CLKCFG_FSEL field. HFRC is the default clock source. Quiesce clock option available.
	I^2S NCO Clock	Variable up to 100 MHz	• EXT_REFCLK (up to 100 MHz) • RF_XTAL_HS (48 MHz) • HFRC/HFAdj (96 MHz) • PLL FOUTPOSTDIV (up to 100MHz)	Supported CRM dividers: 1 - 32.
	I^2S Bus Clock	48MHz, 96 MHz	• HFRC48 • HFRC	
WDT	Ref Clock	0.055, 0.88, 14 and 112 Hz	• 112 Hz: LFRC/8 • 14 Hz: LFRC/64 • 0.88 Hz: LFRC/1024 • 0.055 Hz: LFRC/16384	LFRC source clock is nominally 900 Hz.
	Bus Clock		• HFRC_48MHz	

Table 13: Module Clocks and Dividers

Module / Subsystem	Clock Node	Frequency	Source / Frequency Selections	Additional Requirements / Comments
Timers	Source Clocks	Variable	• HFRC_DIV4, HFRC_DIV16, HFRC_DIV64, HFRC_DIV256, HFRC_DIV1024, HFRC_DIV4096 • LFRC, LFRC_DIV32, LFRC_DIV1024 • 32 kHz XT: XT (uncalibrated), XT_DIV4/DIV16/DIV32/DIV64/DIV128/DIV1024 • RTC_100HZ • TMR00, TMR01 - TMR150, TMR151 • GPIO00 - GPIO99 • BUCKC, BUCKF, BUCKS, BUCKC_LV • XTHS_EXTREF_CLK, XTHS_EXTREF_CLK_DIV2/DIV4/DIV8 • PLLVCO_POSTDIV • RF_XTAL, RF_XTAL_DIV2/DIV4	LFRC source clock is nominally 900 Hz.
	Bus Clock	48 MHz	• HFRC_DIV2	
IOS	IOS I/O Clock 0.75 - 48 MHz	Variable 750 kHz - 48 MHz	• Externally sourced	Sourced from external manager
	Bus Clock	96 MHz	• HFRC	
IOM	IOM I/O Clock	Variable 750 kHz - 24 MHz	• HFRC_24MHZ • HFRC_12MHZ • HFRC_6MHZ • HFRC_3MHZ • HFRC_1p5MHZ • HFRC_750KHz	
	Bus Clock	96 MHz	• HFRC	
I3C	SCL_OUT	10 kHz - 12.5 MHz	• I3C_REF_CLK	I3C PHY digital front-end to analog front-end
	I3C_IN	10 kHz - 12.5 MHz	• External	I3C PHY analog front-end to digital front-end
	I3C_REF_CLK	48 MHz	• HFRC	
	Bus Clock	96 MHz	• HFRC	
UART	UART HF Clock	Variable up to 100 MHz	• HFRC with HFAdj • PLL FOUTPOSTDIV (up to 100 MHz)	Supported CRM dividers: 1 - 32.
	Bus Clock	96 MHz	• HFRC	
GPIO	Bus Clock	48 MHz	• HFRC_DIV2	
PWRCTRL	Bus Clock	48 MHz	• HFRC_DV2	Always ON, asynchronous with CPU/PMU.

Table 13: Module Clocks and Dividers

Module / Subsystem	Clock Node	Frequency	Source / Frequency Selections	Additional Requirements / Comments
Debug	TPIU Clock	192 MHz 96MHz	• HFRC oscillator clk • HFRC_96MHz	Central TPIU TRACECLKIN (TRACECLK is generated by TPIU as 1/2 TRACECLKIN). Asynch, but TRACECLKIN should match the maximum CPU frequency if tracing the CPU. The frequency is controlled by the DBGTPIUCLKSEL in DBGCTRL Register. Gated when not in use.
	Debug Subsystem Clock	192 MHz 96 MHz	• HFRC oscillator clock • HFRC	DBGCLK is synchronous with the CPU clock. If new CPU frequencies are added, they must be added here as well. Gated when not in use
	SWD Clock	100 MHz	• External (Pad Input)	SWJ input clock on the DAP. Tools support up to 100 MHz interface.
ADC	ADC Clock	Variable up to 50 MHz	• HFRC • PLLFPOSTDIV (up to 100 MHz)	Supported CRM dividers: 1 - 32.
MCUCTRL	Bus Clock	24 MHz	• HFRC_24MHz	
RSTGEN	Bus Clock	24 MHz	• HFRC_24MHz	

8.4 Additional Information

Please refer to the CLKGEN registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

9. Real Time Clock (RTC)

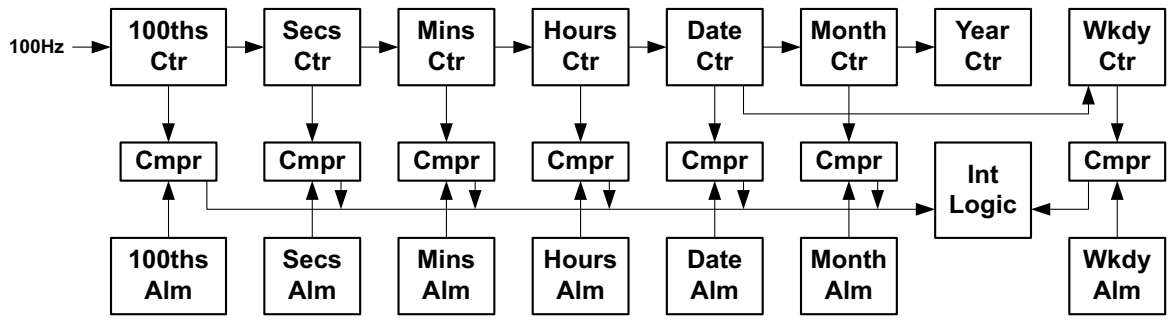

Figure 13. Block diagram for the Real Time Clock Module

9.1 Features

The Real Time Clock (RTC) Module, shown in Figure 13, provides an accurate means of maintaining real time. The Apollo510 Lite SoC has three identical instances of the RTC, each intended for use for the following functions:

- Non-secure domain for use by the non-secure RTOS
- Secure domain for use by the trusted execution environment
- Network subsystem for exclusive use by that subsystem

The security of the RTC modules is determined by the setup of the SAU partitions in the peripheral space.

Key features are:

- 100th of a second resolution
- Time is measured for the years between 1900 and 2199
- Automatic leap year calculation
- Hours are specified in 24 hour mode
- Alarm precise to 1/100 second
- Alarm interval every 100th second, second, minute, hour, date, day of the week or month
- 100 Hz input clock taken from either the high accuracy XT Oscillator or the low power LFRC Oscillator

9.2 Functional Overview

Real time is held in a set of eight Calendar Counters, which hold the following counts of current units in BCD format:

- 1/100th of a second (RTC_CTRLOW_CTR100)
- Second (RTC_CTRLOW_CTRSEC)
- Minute (RTC_CTRLOW_CTRMIN)
- Hour (RTC_CTRLOW_CTRHR)
- Date (RTC_CTRUP_CTRDATE)
- Day of the week (RTC_CTRUP_CTRWKDY)
- Month (RTC_CTRUP_CTRMO)
- Year (RTC_CTRUP_CTRYR)

The timer chain which generates the 100 Hz clock is reset to 0 whenever any of the Calendar Counter Registers is written. Since unintentional modification of the calendar counters is a serious problem, the

RTC_RTCCTL_WRTC bit must be set in order to write any of the counters. Software may stop the clock to the calendar counters by setting the RTC_RTCCTL_RSTOP bit.

The RTC includes special logic to help ensure that the calendar counters may be read reliably, i.e., that no rollover has occurred. Two 32-bit reads are required to read the complete set of counters.

There are seven alarm register fields in the ALMLOW and ALMUP registers which may be used to generate an alarm interrupt at a specific time. These fields correspond to the above listed time calendar counters except for year which does not have an associated alarm. When all selected counters match their corresponding alarm register, the ALM interrupt flag is set.

By setting the Century Enable Bit (RTC_CTRUP_CEB), the Century Bit (RTC_CTRUP_CB) indicates the current century. A value of 0 indicates the 21st century, and a value of 1 indicates the 20th or 22nd century.

The Weekday Counter is a 3-bit counter which counts up to 6 and then resets to 0. It is the responsibility of software to assign particular days of the week to each counter value.

9.3 Additional Information

Please refer to the RTC registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

10. Counter/Timer (TIMER)

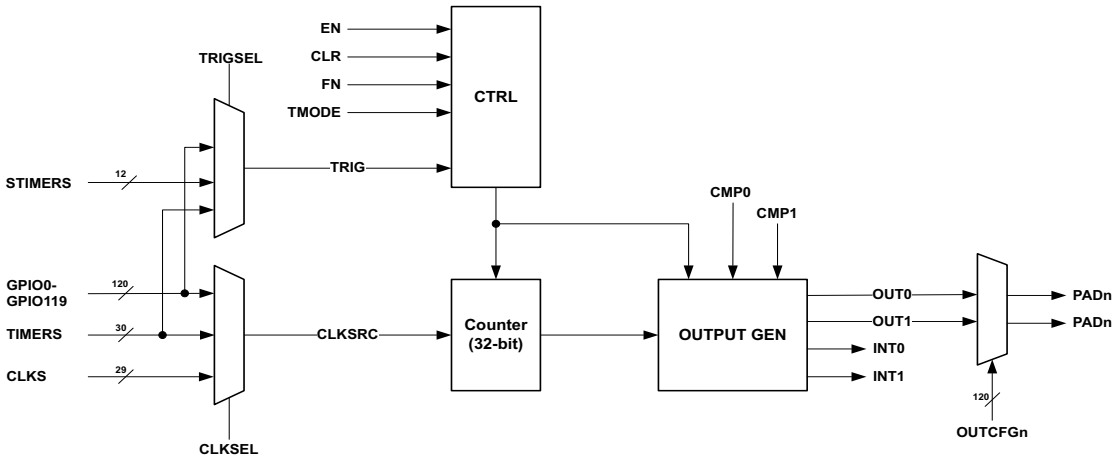

Figure 14. TIMER Block Diagram

NOTE

GPIOs available to be selected as timer triggers and clocks are dependent upon specific device and package pinout. Numbers shown are platform maximums.

10.1 Features

The Apollo510 Lite Series SoCs have the following Timer/Counter instances:

- An instance with sixteen timer/counters for non-secure use
- An instance with four timer/counters for secure use

These counter/timers are in addition to a system timer as described in the System Timer chapter.

Each Timer/Counter includes a very low power asynchronous 32-bit counter and each has external (GPIO) pin connectivity for outputs for each of the two comparators.

The Counter/Timer Module (TIMER) includes features shown in Figure 14 and listed below.

- Sixteen 32-bit binary up-counters used for simple waveform generation, interrupt sources, and counting applications.
- Each timer core has 2 interrupts, TMRnINT0/TMRnINT1 (Only for EDGE, UPCNT and PWM).
  - TMRnINT0 is generated when the value of the TIMER matches the TMRnCMP0 value.
  - TMRnINT1 is generated when the value of the TIMER matches the TMRnCMP1 value.
- For all modes CMP0 defines the end of a counter cycle and the timer will either stop or repeat. CMP1 is a secondary comparator.
- Each timer has two outputs which are controlled from CMP0 and CMP1 registers based on timer mode.
- Each timer is fully independent but can be linked by clocking one timer from another's output.
- Each timer offers several clock options including CLKGEN clocks, another timer output, or any GPIO input.
- Each timer has an interface to the GPIO module which allows any GPIO to be driven by any timer output and any GPIO to be used as a timer input.

- The start of a timer can optionally be triggered by a rising, falling or either edge of another timer output, an STIMER capture/compare event, or any GPIO input.
- Counter register value may be written directly.
- Either or both OUT0/OUT1 outputs of any timer can be inverted by using the POL0/POL1 bit.
- TMRnLMT register can be used to generate 1-255 repetitions of a waveform (0=unlimited).

10.2 Functional Overview

The Apollo510 Lite SoC's Timer/Counter module includes sixteen Timer/Counters, one of which is shown in the Figure 14. This is in addition to a system timer as described in the System Timer chapter. Each Timer/Counter includes a very low power asynchronous 32-bit counter. Each Timer/Counter has external pin connections using any GPIO pads as outputs for each of the two comparators.

Timer functions include those listed in Table 14.

Table 14: Timer Modes

Mode	Outputs	Description/Uses
EDGE	OUT0 transitions when TIMERn = CMP0. OUT1 transitions when TIMERn = CMP1 (if CMP1 < CMP0).	Edge generation (0x1): TIMERn counts up from 0 to CMP0 and stops. A single edge is generated on OUT0 when TIMERn reaches CMP0. If CMP1 < CMP0, then a single edge is also generated on OUT1 when TIMERn reaches CMP1. If CMP0 < CMP1, then no edge is generated on OUT1 (because TIMERn never reaches CMP1). TMRnLMT: Has no effect in this mode. Trigger: Timer does not start until trigger occurs (if enabled). Subsequent triggers ignored.
UPCOUNT	OUT0 pulses for 1 clock cycle when TIMERn = CMP0; counter resets to 0; repeats per TMRnLMT setting. OUT1 pulses for 1 clock cycle when TIMERn = CMP1 (if CMP1 < CMP0).	Repeatable Up-counter (0x2): Counts up from zero to CMP0 and stops (TMRnLMT = 1), repeats N times (TMRnLMT = 2 - 255), or repeats indefinitely until TMRnEN is cleared (TMRnLMT = 0). Timer outputs will be a pulse of one source clock period on the output when the TIMER reaches the associated CMP value. If CMP1 < CMP0, then a single pulse of one source clock period is also generated on OUT1 when TIMERn reaches CMP1. If CMP0 < CMP1, then no pulse is generated on OUT1 (because TIMERn never reaches CMP1). Trigger: Timer does not start until trigger occurs (if enabled). Subsequent triggers ignored.

Table 14: Timer Modes

Mode	Outputs	Description/Uses
PWM	OUT0 transitions when TIMERn = CMP1, then transitions again when TIMERn = CMP0; repeats per TMRnLMT setting. OUT1 is the complement of OUT0.	Repeatable PWM (0x4): Counts up from zero to CMP0 and stops (TMRnLMT=1), repeats N times (TMRnLMT = 2 - 255), or repeats indefinitely (TMRnLMT = 0). CMP0 specifies the period and CMP1 specifies number of TIMERn counts for the initial phase of the output waveform. Trigger: Timer does not start until trigger occurs (if enabled). Subsequent triggers ignored.
SINGLEPATTERN	For TMRnLMT < 32 and for TIMERn count = 0 to TMRnLMT: OUT0 = CMP0[TIMERn]. OUT1 = CMP1[TIMERn]. For TMRnLMT between 32 and 63 (maximum 64-bit pattern consisting of CMP1:CMP0) and for TIMERn count = 0 to TMRnLMT: OUT0 = OUT1 = CMP1:CMP0[TIMERn]. OUT1 can be configured to be the complement of OUT0.	Single-run Pattern Generation (0xC): CMP0 and CMP1 are bit-shifted to form the output pattern on OUT0 and OUT1, or concatenation of CMP1:CMP0 is bit shifted to form the output pattern on both OUT0 and OUT1. The TIMER count is an up-counter that indexes into the bits of CMP0 (TIMER values from 1-31) and CMP1 (TIMER values 32-63). TMRnLMT value defines the length of the pattern minus 1 (0 = 1-bit pattern, 63 = 64-bit pattern). OUT1 is the same as OUT0, but can be inverted for motor control applications. INT0 is triggered when all TMRnLMT+1 bits have been streamed out. INT1 is triggered only when TMRnLMT is set to 31 and all 32 bits of CMP0 have been streamed out. Trigger: Timer does not start until trigger occurs (if enabled). After clearing and reconfiguring the timer for this mode, a subsequent trigger restarts the pattern replay.
REPEATPATTERN	For TMRnLMT < 32 and for TIMERn count = 0 to TMRnLMT: OUT0 = CMP0[TIMERn]. OUT1 = CMP1[TIMERn]. For TMRnLMT between 32 and 63 (maximum 64-bit pattern consisting of CMP1:CMP0) and for TIMERn count = 0 to TMRnLMT: OUT0 = OUT1 = CMP1:CMP0[TIMERn]. OUT1 can be configured to be the complement of OUT0.	Repeated Pattern Generation (0xD): CMP0 and CMP1 are bit-shifted to form the output pattern on OUT0 and OUT1 as described in SINGLEPATTERN mode with the exception that the timer repeats the pattern after TMRnLMT+1 bits have been streamed out, resetting TMRnLMT back to 0 after each iteration. Since TMRnLMT is used for the repeat pattern length, there is no option to repeat the pattern N times. The iterations repeat indefinitely until TIMERn is disabled.

NOTE

CMP0/CMP1 values should not be changed when the TIMER is running or else it will corrupt the counter.

Software should assert TMRnCLR each time before asserting TMRnEN. if this is not done, stale values will remain.

10.3 Additional Information

Please refer to the TIMER registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

11. System Timer (STIMER)

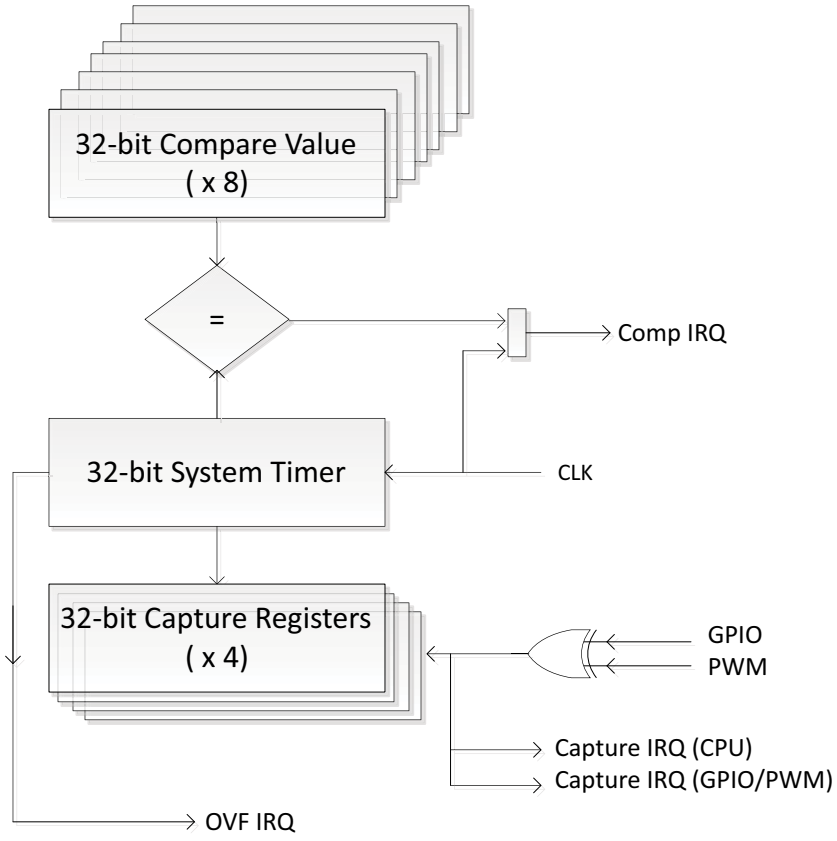

Figure 15. STIMER Block Diagram

11.1 Features

The System Timer (STIMER) includes features shown in Figure 15 and listed below.

- 32-bit binary counter used for RTOS scheduling decisions
- Eight 32-bit compare and interrupt registers to facilitate light weight scheduling (designs without RTOS)
- Accurate scheduling of comparator interrupts
- Only offsets from “NOW” written to comparator registers
- Maintains real time epoch for applications
- Overflow interrupt to allow firmware to keep the extended part (more than 32-bits) of real time epoch
- Time stamping hardware for multiple sensor streams (4 capture registers)
- Firmware handling of odd calculations such as Leap Second and events like surprise/legislated changes to the daylight savings time transition dates
- Firmware handling of 1024 versus 1000 scaling of real time conversions
- Only reset by POA (Power On Analog - system cold reset) so that it retains time across all POI and POR (system warm reset) events except full power cycles
- Contains three 32-bit NVRAM registers that are only reset by POA to maintain real time offset from epoch
- Programmable external GPIO trigger and/or PWM trigger on capture (required for sensor synchronization)

11.2 Functional Overview

The System Timer tracks the global synchronized counter. It can be used for RTOS scheduling and real-time system tracking. This timer is provided in addition to the other timer peripherals to enable software/ firmware to have a simple, globally synchronized timer source.

The System Timer Module provides real time measurement for all task scheduling, sensor sample rate calibration, and tracking of real time and calendar maintenance. To do this the STIMER maintains a continuously running 32-bit counter that increments at the selected clock rate. The counter is only reset by a POA (Power On Analog) event, ensuring that time is preserved across system warm resets.

Eight Compare Registers (SCMPR0-SCMPR7) allow firmware to schedule events relative to the current time. When writing to a compare register, firmware writes an offset value (delta) from the current counter value. The hardware automatically adds this offset to the current STTMR value and updates the SCMPRn register with the absolute compare value.

Four Capture Registers provide hardware time stamping for sensor synchronization. These registers can be triggered by external GPIO events or PWM signals, enabling precise correlation of multiple sensor data streams with the system timeline.

There are three 32-bit NVRAM Registers which are provided to maintain real-time offset information across power cycles. These registers are only reset by POA, allowing firmware to reconstruct the full time and date after any reset event except a complete power loss.

The STIMER offers several clock sources. Clock selection is done via the STCFG_CLKSEL bit field. Available clock sources include:

- Low-frequency oscillator (LFRC or LFXTAL) for low-power operation
- High-frequency clock options for higher timing resolution

11.3 Additional Information

Please refer to the STIMER registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

12. Watchdog Timer (WDT)

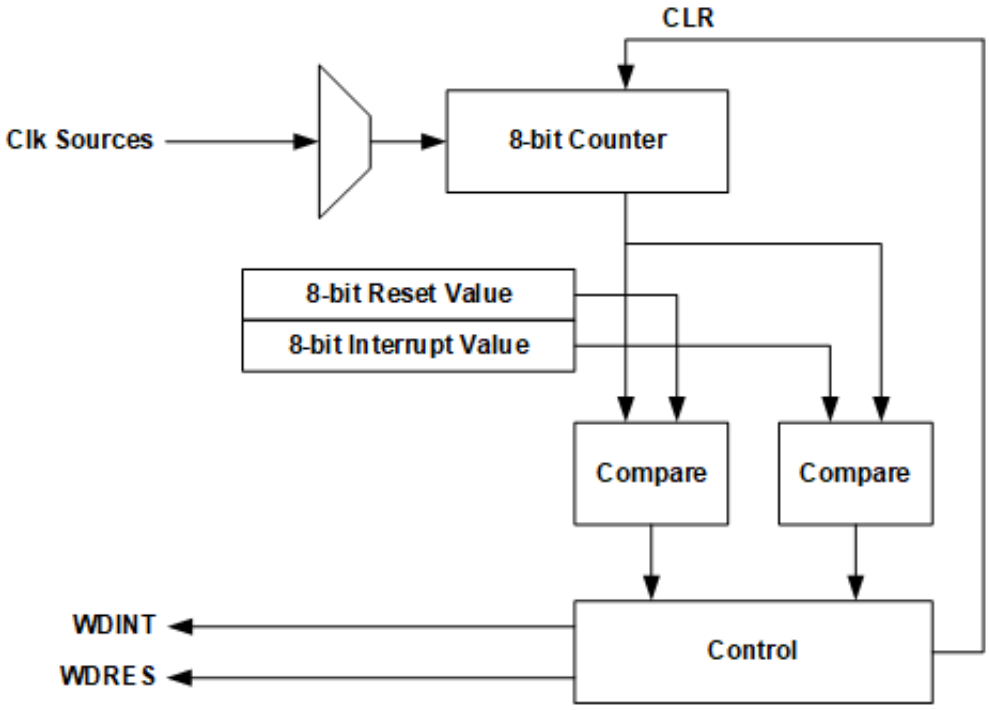

Figure 16. Watchdog Timer Block Diagram

12.1 Features

The Watchdog Timer (WDT) includes features shown in Figure 16 and listed below.

- Ensures software remains operational by initiating a reset if WDT times out.
- May be clocked by one of four selectable prescalers of the LFRC clock.
- May be locked to ensure software cannot disable its functionality.
- Early warning may be implement via an interrupt.

12.2 Functional Overview

The Watchdog Timer (WDT) is used to ensure that software is operational, by resetting the Apollo510 Lite SoC if the WDT reaches a configurable value before being cleared by software. The WDT can be clocked by one of four selectable prescalers of the always active low-power LFRC clock, but is nominally clocked at 128 Hz. The WDT may be locked to ensure that software cannot disable its functionality, in which case the WDTCFG register cannot be accidentally reprogrammed. An interrupt can also be generated at a different counter value to implement an early warning function. When the WDTCFG_NMIEN bit is set, the watchdog timeout will trigger a NMI.

NOTE: The RESEN bit in the WDTCFG register must be set and the WDREN bit in the RSTCFG register must be set to enable a watchdog timer reset condition.

A second WDT is included on the Apollo510 Lite SoC in order for these two WDTs to support the secure and non-secure domains. The functionality of the two WDTs is identical, and each can reset the MCU. It is expected that one WDT will be mapped into the non-secure peripheral address space, and the other into the secure peripheral address space.

An additional WDT has been added for the Cortex-M4 based Network Subsystem. The functionality of this WDT is identical to the others except that it only resets the Network Subsystem.

12.3 Additional Information

Please refer to the WDT registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

13. General Purpose Input/Output (GPIO)

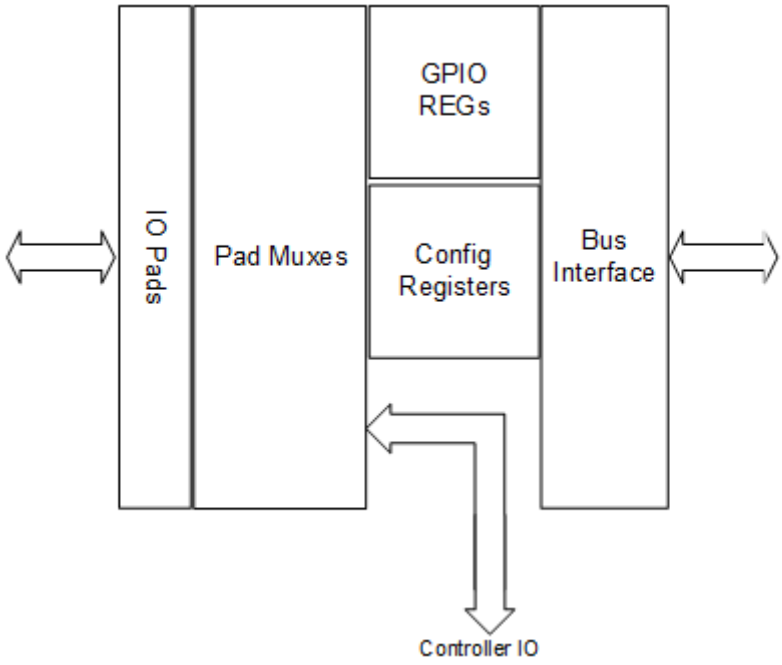

Figure 17. Block Diagram for the General Purpose Input/Output (GPIO) Module

13.1 Features

The GPIO module can be represented as shown in the block diagram in Figure 17.

Key features include the following:

- Up to 120 GPIOs depending on derivative and package
- Six selectable I/O voltage domains depending on derivative and package (applies to set of GPIOs)
- 8 programmable GPIO interrupt groups
- Flexible GPIO Controls
  - 50 kΩ pull-down and 1.5 kΩ to 100 kΩ pull-up resistors
  - Multiple drive strengths
  - Multi-edge interrupts
  - Up to 12 function selects per GPIO
  - Grouped or masked interrupts
  - Configurable output drive mode (push-pull, open drain, tri-stated push-pull modes)

13.2 Functional Overview

The Apollo510 Lite SoC's General Purpose I/O and Pad Configuration (GPIO) Module controls connections to up to 120 digital/analog pads. Each pad may be connected to a variety of module interface signals, with all pad input and output selection and control managed by the GPIO module. In addition, any pad may function as a general purpose input and/or output pad to be configured for a variety of external functions. Each GPIO may be configured to generate an interrupt when a transition occurs on the input.

For the Apollo510 Lite SoC, any GPIO pad brought out to an external pin may be configured as a chip enable for any IOM or for the Display Controller. Pins available as chip enables for MSPI instances are as specified starting in Table 16. The pins available for specific MSPI chip enables are shown as function

selections with a “MNCEx_y” entry (orange), where x is the MSPI instance and y is the chip select number for that instance.

13.2.1 High-Speed Pads

There are several high-speed GPIO available for use on the SoC - GPIO0-4, 35-39, 65-77, 81 and 112[1]. These GPIO pads, which may serve as high-speed interfaces (MSPI, TPIU), are supplied by voltage rails as specified and described in section 13.4, and support a range of voltage levels as specified in the “External Voltage Supplies” table of the Electrical Characteristics chapter. These high-speed pads have the following characteristics and settings:

- Capacitive load: 15 pF
- High-speed mode for fastest performance (by using internal low-voltage devices)
- Drive Strength options:
  - PVT1 - ODT 50 Ω (PVT1_ODT50OHM)[2]
  - PVT2 - ODT 50 Ω (PVT2_ODT50OHM)
  - PVT3 - ODT 50 Ω (PVT3_ODT50OHM)
  - Drive ODT 0 Ω (ODT_0OHM)
- Pull-up/pull-down options:
  - 50 kΩ pull-up
  - 50 kΩ pull-down

NOTE

The GPIO_PINCFGn_SRn field for high-speed pads is used to set the pad speed grade: 0 = Normal, 1 = Fast (recommended).

NOTE

The Drive Strength setting (GPIO_PINCFGn_DSn) for high-speed pads is set as the on-die termination (ODT) setting for the pad. This setting is intended for production trimming on high-speed pads and should only be changed from the default by the user in special cases to mitigate PCB-specific signal integrity issues.

13.3 GPIO Interrupts

The Apollo510 Lite SoC architecture has GPIO interrupts in two groups: 0-3 and 4-7. 0-3 are groups of 32 GPIO interrupts, and 4-7 form the second group. Each interrupt is enabled, disabled, cleared or set with a standard set of interrupt registers GPIO_MCUN0INTnEN, GPIO_MCUN0INTnSTAT, GPIO_MCUN0INTnCLR and GPIO_MCUN0INTnSET, where n = 0 to 3 for GPIO pads 0 to 31, 32 to 63, 64 to 95, and 96 to 119, respectively[3]. The N0 designation in these registers indicates that these are interrupt register set 0. A duplicate set of registers, with a designation N1, is available and these registers are similarly named GPIO_MCUN1INTnEN, GPIO_MCUN1INTnSTAT, GPIO_MCUN1INTnCLR and GPIO_MCUN1INTnSET. The purpose of this dual set of registers is to enable segregation of an interrupt,

1. GPIO112 not pinned out on CSP package.
2. PVT - process/voltage/temperature; ODT - on-die termination. On-die termination is controlled by drive strength control bits in the GPIO_PINCFGn_DSn field.
3. Bits used in the GPIO_MCUNmINTn registers depend on the pads used by the specific SoC derivative and package. See the available pads for each package in the Pin Mapping table later in this chapter.

or a small set of interrupts, which may have higher importance and thus should be handled at a higher priority level and/or with minimal latency.

13.4 Pad Configuration Functions

Each GPIO on a Apollo510 Lite SoC package can be configured as one of several functions according to the Pin Mapping tables starting with Table 16. Functions are grouped by module per the color coding shown in Table 18.

The I/O voltage source reference for each pad as listed in the “I/O Voltage” column of the Pin Mapping tables equates to the corresponding voltage supply shown in Table 15. See the Electricals “External Voltage Supplies” section for specified voltage range for each supply.

Table 15: I/O Pin Voltage Source

I/O Voltage Reference	Voltage Supply	Description	GPIO Powered	Modules Powered[1]
0	VDDH	Primary Unregulated Logic Supply (No I/O on this rail)	-	-
1	VDDH1	Alternate I/O Supply (Primary Interface is TRACE)	GPIO0-4, 28, 40, 42, 47-52, 113	DC, IOS, MSPI1, SWTRACE
2	VDDH2	Primary I/O Supply, OTP	GPIO5-21, 25-27, 29-34, 41, 53-58, 80, 82-87, 102-109, 114-118	ADC, DBIB, IOM, MSPI2, (PDM)I2S, SDIO, SWTRACE, VCOMP
3	VDDH3	Alternate I/O Supply (Primary Interface is MSPI0/MSPI2 high speed)	GPIO35-39, 65-79, 81, 110-112	MSPI0, MSPI2, SWTRACE
4	VDDH4	Alternate I/O Supply (Primary Interface is SDIO1/eMMC1)	GPIO43-46, 59-64	(PDM)I2S, SDIO
5	VDDH5	Alternate I/O Supply (Primary Interface is MIP display)	GPIO22-24, 88-101, 119	DBIB, IOM

1. All pads selected for any specific interface must be at the same voltage level.

There are two core voltage designations for the GPIOs, 0 and 1, which specify the “Wake State” they can support. Core voltage 0 is in an always-on / wake-capable domain in the S_{DS3} ("deeper" sleep) System Power State. There are 16 always-on GPIOs which can be used to wake when in the deeper sleep mode powered by core voltage 0: GPIO5, 6, and 8 - 21. All GPIOs can be powered by core voltage 1 in a domain that is switched / wake-capable in deep sleep power state S_{DS2} or higher.

NOTE

For the "deeper" sleep mode (S_{DS3}), software must program the respective DSPULLCFG bits in the GPIO PINCFG register to set the pull-up or pull-down state for each pin to ensure proper state when entering deeper sleep. The DSPULLCFG bits only apply to the GPIOs that get powered down in this mode (all but the 16 always-on GPIOs). These fields are marked RESERVED in the registers of the always-on GPIOs.

NOTE

The Secure Bootloader (SBL) uses GPIO28 as the SWO output (1 Mbaud) to make bootup status/information available to the user. This pin is configured as an output and will toggle during bootup. Care should be taken by the user when connecting this pin to an external peripheral.

Table 16: Apollo510 Lite SoC Pin Mapping (Pg 1)

Pad	PADnFNCSEL												BGA Pkg	CSP Pkg	I/O Voltage
	0	1	2	3	4	5	6	7	9	10	12	13			
0	SWTRACECLK	SLFDSCK	DISP_QSPI_D0	GPIO0	DISP_SPI_SD	DISP_SPI_SDO	CT0	NCE0	-	-	SLFDSCL	DISP_QSPI_D0_OUT	X	X	1
1	SWTRACE0	SLFDMOSI	DISP_QSPI_D1	GPIO1	DISP_SPI_DCX	-	CT1	NCE1	UART0_TX	UART1_CTS	SLFDSDAWIR3	-	X	X	1
2	SWTRACE1	SLFDMISO	DISP_QSPI_SCK	GPIO2	DISP_SPI_SCK	-	CT2	NCE2	UART0_RX	UART1_RTS	XT_EXT	-	X	X	1
3	SWTRACE2	SLFDnCE	DISP_QSPI_D2	GPIO3	DISP_SPI_SDI	-	CT3	NCE3	-	-	-	-	X	X	1
4	SWTRACE3	SLFDINT	DISP_QSPI_D3	GPIO4	DISP_SPI_RST	-	CT4	NCE4	UART1_TX	UART0_CTS	-	-	X	X	1
5	M0SCL	M0SCK	PDMI2S0_SDOUT	GPIO5	-	32KHzXT	CT5	NCE5	UART1_RX	UART0_RTS	I2S0_SDOUT	I2S0_DATA	X	X	2
6	M0SDAWIR3	M0MOSI	PDMI2S0_WS	GPIO6	CLKOUT	-	CT6	NCE6	UART0_TX	UART1_CTS	I2S0_WS	-	X	X	2
7	M0MISO	VCMPO	-	GPIO7	TRIG0	-	CT7	NCE7	UART0_RX	UART1_RTS	I2S0_SDIN	-	X	X	2
8	CMPRF1	M1SCL	M1SCK	GPIO8	TRIG1	-	CT8	NCE8	UART1_TX	UART0_CTS	-	-	X	X	2
9	CMPRF0	M1SDAWIR3	M1MOSI	GPIO9	TRIG2	-	CT9	NCE9	UART1_RX	UART0_RTS	-	-	X	X	2
10	CMPIN0	M1MISO	PDMI2S0_CLK	GPIO10	TRIG3	-	CT10	NCE10	UART0_TX	UART1_CTS	I2S0_CLK	-	X	X	2
11	CMPIN1	-	PDMI2S0_CLK	GPIO11	TRIG0	-	CT11	NCE11	UART0_RX	UART1_RTS	I2S0_CLK	-	X	X	2
12	ADCSE7	-	PDMI2S0_WS	GPIO12	TRIG1	CMPRF2	CT12	NCE12	UART1_TX	UART0_CTS	I2S0_WS	-	X	X	2
13	ADCSE6	-	PDMI2S0_SDOUT	GPIO13	TRIG2	-	CT13	NCE13	UART1_RX	UART0_RTS	I2S0_SDOUT	I2S0_DATA	X	X	2
14	ADCSE5	-	-	GPIO14	TRIG3	-	CT14	NCE14	UART0_TX	UART1_CTS	I2S0_SDIN	-	X	X	2
15	ADCSE4	REFCLK_EXT	-	GPIO15	TRIG0	-	CT15	NCE15	UART0_RX	UART1_RTS	-	-	X	X	2
16	ADCSE3	-	-	GPIO16	TRIG1	-	CT16	NCE16	UART0_TX	UART1_CTS	-	-	X	X	2
17	ADCSE2	-	-	GPIO17	TRIG2	-	CT17	NCE17	UART0_RX	UART1_RTS	-	-	X	X	2
18	ADCSE1	-	-	GPIO18	TRIG3	-	CT18	NCE18	UART1_TX	UART0_CTS	-	-	X	X	2
19	ADCSE0	-	-	GPIO19	TRIG0	-	CT19	NCE19	UART1_RX	UART0_RTS	-	-	X	X	2
20	SWDCK	-	-	GPIO20	TRIG1	-	CT20	NCE20	UART1_TX	UART0_CTS	-	-	X	X	2
21	SWDIO	-	-	GPIO21	TRIG2	-	CT21	NCE21	UART1_RX	UART0_RTS	-	-	X	X	2
22	M5SCL	M5SCK	-	GPIO22	TRIG3	SWO	CT22	NCE22	UART0_TX	UART1_CTS	RF_XCVR_TST0	-	X	X	5
23	M5SDAWIR3	M5MOSI	BTDM_RXEN	GPIO23	TRIG0	SWO	CT23	NCE23	UART0_RX	UART1_RTS	ST_WCI_2W_RXD	-	X	X	5
24	M5MISO	-	BTDM_TXEN	GPIO24	TRIG1	SWO	CT24	NCE24	UART1_TX	UART0_CTS	ST_WCI_1W_RXD	ST_WCI_2W_TXD	X	X	5
25	M2SCL	M2SCK	VCMPO	GPIO25	TRIG2	-	CT25	NCE25	UART1_RX	UART0_RTS	-	-	X	X	2
26	M2SDAWIR3	M2MOSI	-	GPIO26	TRIG3	SWTRACECTL	CT26	NCE26	UART0_TX	UART1_CTS	-	-	X	X	2
27	M2MISO	I2S0_MCLK	VCMPO	GPIO27	TRIG0	-	CT27	NCE27	UART0_RX	UART1_RTS	-	-	X	X	2
28	SWO	SWTRACECTL	-	GPIO28	TRIG1	-	CT28	NCE28	UART1_RX	UART0_RTS	-	-	X	X	1
29	M3SCL	M3SCK	-	GPIO29	TRIG2	-	CT29	NCE29	UART1_TX	UART0_CTS	I2S0_SDIN	-	X	X	2
30	M3SDAWIR3	M3MOSI	PDMI2S0_SDOUT	GPIO30	TRIG3	-	CT30	NCE30	UART0_TX	UART1_CTS	I2S0_SDOUT	I2S0_DATA	X	X	2
31	M3MISO	CLKOUT	PDMI2S0_WS	GPIO31	TRIG0	COEX_GRANT	CT31	NCE31	UART0_RX	UART1_RTS	I2S0_WS	-	X	X	2
32	M4SCL	M4SCK	-	GPIO32	TRIG1	COEX_REQ	CT32	NCE32	UART1_TX	UART0_CTS	-	-	X	X	2
33	M4SDAWIR3	M4MOSI	-	GPIO33	TRIG2	COEX_PRIORITY	CT33	NCE33	UART1_RX	UART0_RTS	-	-	X	X	2
34	M4MISO	SWO	-	GPIO34	TRIG3	COEX_FREQ	CT34	NCE34	UART0_TX	UART1_CTS	-	-	X	X	2
35	MSPI0_8	SWTRACECLK	-	GPIO35	-	-	CT35	NCE35	UART0_RX	UART1_RTS	-	-	X	X	3
36	MSPI0_0	SWTRACE0	-	GPIO36	-	-	CT36	NCE36	UART1_TX	UART0_CTS	-	-	X	X	3
37	MSPI0_1	SWTRACE1	-	GPIO37	-	32KHzXT	CT37	NCE37	UART1_RX	UART0_RTS	-	-	X	X	3
38	MSPI0_2	SWTRACE2	-	GPIO38	-	-	CT38	NCE38	-	-	-	-	X	X	3
39	MSPI0_3	SWTRACE3	-	GPIO39	-	-	CT39	NCE39	-	-	-	-	X	X	3
40	MNCE1_0	-	-	GPIO40	-	-	CT40	NCE40	UART1_TX	UART0_CTS	-	-	X		1
41	MNCE2_0	-	-	GPIO41	-	-	CT41	NCE41	UART1_RX	UART0_RTS	-	-	X		2
42	MNCE1_1	DISP_TE	-	GPIO42	ST_WCI_1W_RXD	ST_WCI_2W_TXD	CT42	NCE42	-	-	BTDM_RXEN	-	X		1
43	-	SDIF1_DAT4	COEX_GRANT	GPIO43	PDMI2S0_SDOUT	-	CT43	NCE43	UART1_TX	UART0_CTS	I2S0_SDOUT	I2S0_DATA	X	X	4
44	-	SDIF1_DAT5	COEX_REQ	GPIO44	PDMI2S0_WS	SWO	CT44	NCE44	UART1_RX	UART0_RTS	I2S0_WS	-	X	X	4
45	-	SDIF1_DAT6	COEX_PRIORITY	GPIO45	-	32KHzXT	CT45	NCE45	UART1_TX	UART0_CTS	I2S0_SDIN	-	X	X	4
46	I2S0_MCLK	SDIF1_DAT7	COEX_FREQ	GPIO46	TRIG3	SWO	CT46	NCE46	UART1_RX	UART0_RTS	-	-	X	X	4
47	MSPI1_4	SWTRACECLK	CLKOUT	GPIO47	TRIG0	-	CT47	NCE47	-	-	-	-	X		1
48	MSPI1_0	SWTRACE0	CLKOUT	GPIO48	TRIG1	-	CT48	NCE48	UART0_TX	UART1_CTS	-	-	X		1
49	MSPI1_1	SWTRACE1	-	GPIO49	TRIG2	-	CT49	NCE49	UART0_RX	UART1_RTS	-	-	X		1
50	MSPI1_2	SWTRACE2	-	GPIO50	TRIG3	-	CT50	NCE50	UART1_TX	UART0_CTS	-	-	X		1
51	MSPI1_3	SWTRACE3	-	GPIO51	TRIG0	-	CT51	NCE51	UART1_RX	UART0_RTS	-	-	X		1
52	MSPI1_5	SWTRACECTL	CLKOUT	GPIO52	TRIG1	-	CT52	NCE52	UART0_TX	UART1_CTS	-	-	X		1
53	MSPI2_8	-	-	GPIO53	-	SWO	CT53	NCE53	UART0_RX	UART1_RTS	-	-	X		2
54	MSPI2_0	-	32KHzXT	GPIO54	-	-	CT54	NCE54	UART1_TX	UART0_CTS	-	-	X		2
55	MSPI2_1	-	32KHzXT	GPIO55	-	-	CT55	NCE55	UART1_RX	UART0_RTS	-	-	X		2
56	MSPI2_2	-	CLKOUT	GPIO56	-	-	CT56	NCE56	UART0_TX	UART1_CTS	-	-	X		2
57	MSPI2_3	-	CLKOUT	GPIO57	-	-	CT57	NCE57	UART0_RX	UART1_RTS	-	-	X		2
58	MSPI2_9	-	-	GPIO58	-	-	CT58	NCE58	UART1_TX	UART0_CTS	-	-	X		2

Table 17: Apollo510 Lite SoC Pin Mapping (Pg 2)

Pad	PADnFNCSEL												BGA Pkg	CSP Pkg	I/O Voltage
	0	1	2	3	4	5	6	7	9	10	12	13			
59	SDIF1_DAT0	-	-	GPIO59	TRIG2	-	CT59	NCE59	UART1_RX	UART0_RTS	-	-	X	X	4
60	SDIF1_DAT1	-	32KHzXT	GPIO60	TRIG3	SWO	CT60	NCE60	UART0_TX	UART1_CTS	-	-	X	X	4
61	SDIF1_DAT2	-	32KHzXT	GPIO61	TRIG0	SWO	CT61	NCE61	UART0_RX	UART1_RTS	-	-	X	X	4
62	SDIF1_DAT3	-	32KHzXT	GPIO62	TRIG1	SWO	CT62	NCE62	UART1_TX	UART0_CTS	-	-	X	X	4
63	SDIF1_CLKOUT	-	-	GPIO63	TRIG2	SWO	CT63	NCE63	UART1_RX	UART0_RTS	-	-	X	X	4
64	SDIF1_CMD	-	-	GPIO64	TRIG3	SWO	CT64	NCE64	UART0_TX	UART1_CTS	-	-	X	X	4
65	MSPI0_4	-	CLKOUT	GPIO65	-	-	CT65	NCE65	UART0_TX	UART1_CTS	-	-	X	X	3
66	MSPI0_5	-	32KHzXT	GPIO66	-	-	CT66	NCE66	UART0_RX	UART1_RTS	-	-	X	X	3
67	MSPI0_6	-	32KHzXT	GPIO67	-	-	CT67	NCE67	UART1_TX	UART0_CTS	-	-	X	X	3
68	MSPI0_7	-	-	GPIO68	-	SWO	CT68	NCE68	UART1_RX	UART0_RTS	-	-	X	X	3
69	MSPI0_10	-	32KHzXT	GPIO69	MSPI2_0	SWO	CT69	NCE69	UART0_RX	UART1_RTS	-	-	X	X	3
70	MSPI0_11	SWTRACE0	-	GPIO70	MSPI2_1	COEX_GRANT	CT70	NCE70	UART1_TX	UART0_CTS	-	-	X	X	3
71	MSPI0_12	SWTRACE1	-	GPIO71	MSPI2_2	COEX_REQ	CT71	NCE71	UART1_RX	UART0_RTS	-	-	X	X	3
72	MSPI0_13	SWTRACE2	-	GPIO72	MSPI2_3	COEX_PRIORITY	CT72	NCE72	UART0_TX	UART1_CTS	-	-	X	X	3
73	MSPI0_14	SWTRACE3	-	GPIO73	MSPI2_4	COEX_FREQ	CT73	NCE73	UART0_RX	UART1_RTS	-	-	X	X	3
74	MSPI0_15	-	-	GPIO74	MSPI2_5	-	CT74	NCE74	UART1_TX	UART0_CTS	-	-	X	X	3
75	MSPI0_16	-	CLKOUT	GPIO75	MSPI2_6	-	CT75	NCE75	UART1_RX	UART0_RTS	-	-	X	X	3
76	MSPI0_17	-	CLKOUT	GPIO76	MSPI2_7	-	CT76	NCE76	UART0_TX	UART1_CTS	-	-	X	X	3
77	MSPI0_18	-	32KHzXT	GPIO77	MSPI2_9	-	CT77	NCE77	UART0_RX	UART1_RTS	-	-	X	X	3
78	MNCE0_0	-	-	GPIO78	-	-	CT78	NCE78	UART1_TX	UART0_CTS	-	-	X		3
79	MNCE0_1	DISP_TE	ST_WCI_2W_TXD	GPIO79	ST_WCI_1W_RXD	-	CT79	NCE79	UART1_RX	UART0_RTS	BTDM_TXEN	-	X	X	3
80	MNCE2_1	DISP_TE	ST_WCI_2W_TXD	GPIO80	ST_WCI_1W_RXD	-	CT80	NCE80	UART0_TX	UART1_CTS	-	-	X		2
81	MSPI0_9	-	-	GPIO81	-	-	CT81	NCE81	UART0_RX	UART1_RTS	-	-	X	X	3
82	SDIF0_CLKOUT	-	-	GPIO82	TRIG0	-	CT82	NCE82	UART1_TX	UART0_CTS	-	-	X		2
83	SDIF0_DAT0	-	-	GPIO83	TRIG1	-	CT83	NCE83	UART1_RX	UART0_RTS	-	-	X		2
84	SDIF0_DAT1	-	-	GPIO84	TRIG2	-	CT84	NCE84	UART0_TX	UART1_CTS	-	-	X		2
85	SDIF0_DAT2	-	-	GPIO85	TRIG3	-	CT85	NCE85	UART0_RX	UART1_RTS	-	-	X		2
86	SDIF0_DAT3	-	-	GPIO86	TRIG0	-	CT86	NCE86	UART1_TX	UART0_CTS	-	-	X		2
87	SDIF0_CMD	-	-	GPIO87	TRIG1	-	CT87	NCE87	UART1_RX	UART0_RTS	-	-	X		2
88	DISP_ENB	-	32KHzXT	GPIO88	TRIG2	COEX_GRANT	CT88	NCE88	UART0_TX	UART1_CTS	-	DBIB_CSX	X		5
89	DISP_XRST	-	-	GPIO89	TRIG3	COEX_REQ	CT89	NCE89	UART0_RX	UART1_RTS	-	DBIB_DCX	X		5
90	DISP_R1	-	CLKOUT	GPIO90	TRIG0	COEX_PRIORITY	CT90	NCE90	UART1_TX	UART0_CTS	-	DBIB_WRX	X		5
91	DISP_R2	-	CLKOUT	GPIO91	TRIG1	COEX_FREQ	CT91	NCE91	UART1_RX	UART0_RTS	-	DBIB_RDX	X		5
92	DISP_G1	-	DISP_QSPI_D0	GPIO92	TRIG2	DISP_SPI_SD	CT92	NCE92	UART0_TX	UART1_CTS	DISP_SPI_SDO	DISP_QSPI_D0_OUT	X		5
93	DISP_G2	-	DISP_QSPI_D1	GPIO93	TRIG3	DISP_SPI_DCX	CT93	NCE93	UART0_RX	UART1_RTS	-	DBIB_D0	X		5
94	DISP_B1	-	DISP_QSPI_SCK	GPIO94	TRIG0	DISP_SPI_SCK	CT94	NCE94	UART1_TX	UART0_CTS	-	DBIB_D1	X		5
95	DISP_B2	-	DISP_QSPI_D2	GPIO95	TRIG1	DISP_SPI_SDI	CT95	NCE95	UART1_RX	UART0_RTS	RF_XCVR_TST1	DBIB_D2	X		5
96	DISP_HST	-	DISP_QSPI_D3	GPIO96	TRIG2	DISP_SPI_RST	CT96	NCE96	UART0_TX	UART1_CTS	RF_XCVR_TST2	DBIB_D3	X		5
97	DISP_VST	-	-	GPIO97	TRIG3	SWO	CT97	NCE97	UART0_RX	UART1_RTS	RF_XCVR_TST3	DBIB_D4	X		5
98	DISP_HCK	-	-	GPIO98	TRIG0	SWO	CT98	NCE98	UART1_TX	UART0_CTS	-	DBIB_D5	X		5
99	DISP_VCK	-	ST_WCI_2W_RXD	GPIO99	TRIG1	SWO	CT99	NCE99	UART1_RX	UART0_RTS	BTDM_TXEN	DBIB_D6	X		5
100	DISP_TE	ST_WCI_1W_RXD	ST_WCI_2W_TXD	GPIO100	TRIG2	-	CT100	NCE100	UART0_TX	UART1_CTS	BTDM_RXEN	DBIB_D7	X		5
101	DISP_QSPI_CS_N	-	BTDM_TXEN	GPIO101	TRIG3	DISP_SPI_CS_N	CT101	NCE101	UART0_RX	UART1_RTS	ST_WCI_1W_RXD	ST_WCI_2W_TXD	X		5
102	SLFDSCK	SLFDSCL	PDMI2S0_CLK	GPIO102	TRIG0	-	CT102	NCE102	UART1_TX	UART0_CTS	-	DBIB_D8	X		2
103	SLFDMOSI	SLFDSDAWIR3	PDMI2S0_SDOUT	GPIO103	TRIG1	-	CT103	NCE103	UART1_RX	UART0_RTS	-	DBIB_D9	X		2
104	SLFDMISO	BTDM_TXEN	PDMI2S0_WS	GPIO104	TRIG2	-	CT104	NCE104	UART0_TX	UART1_CTS	-	DBIB_D10	X		2
105	SLFDnCE	BTDM_RXEN	-	GPIO105	TRIG3	-	CT105	NCE105	UART0_RX	UART1_RTS	-	DBIB_D11	X		2
106	SLFDINT	I2S0_MCLK	-	GPIO106	TRIG0	ST_WCI_2W_RXD	CT106	NCE106	UART1_TX	UART0_CTS	-	DBIB_D12	X		2
107	PDM0_CLK	-	-	GPIO107	TRIG1	-	CT107	NCE107	UART1_RX	UART0_RTS	-	DBIB_D13	X	X	2
108	PDM0_DATA	-	-	GPIO108	TRIG2	-	CT108	NCE108	UART0_TX	UART1_CTS	-	DBIB_D14	X	X	2
109	I2S0_CLK	PDMI2S0_CLK	-	GPIO109	TRIG3	-	CT109	NCE109	UART0_RX	UART1_RTS	-	DBIB_D15	X		2
110	MNCE2_0	-	-	GPIO110	TRIG0	-	CT110	NCE110	UART1_TX	UART0_CTS	-	-	X	X	3
111	MNCE2_1	-	-	GPIO111	TRIG1	ST_WCI_2W_RXD	CT111	NCE111	UART1_RX	UART0_RTS	BTDM_RXEN	-	X		3
112	MSPI2_8	-	-	GPIO112	TRIG2	-	CT112	NCE112	UART0_TX	UART1_CTS	-	-	X		3
113	DISP_QSPI_CS_N	-	ST_WCI_2W_RXD	GPIO113	TRIG3	DISP_SPI_CS_N	CT113	NCE113	UART0_RX	UART1_RTS	BTDM_TXEN	-	X		1
114	SDIF0_DAT4	-	BTDM_TXEN	GPIO114	TRIG0	-	CT114	NCE114	UART1_TX	UART0_CTS	-	-	X		2
115	SDIF0_DAT5	-	BTDM_RXEN	GPIO115	TRIG1	-	CT115	NCE115	UART1_RX	UART0_RTS	-	-	X		2
116	SDIF0_DAT6	-	-	GPIO116	TRIG2	SWO	CT116	NCE116	UART0_TX	UART1_CTS	-	-	X		2
117	SDIF0_DAT7	-	-	GPIO117	TRIG3	SWO	CT117	NCE117	UART0_RX	UART1_RTS	-	-	X		2
118	I2S0_MCLK	-	PDMI2S0_CLK	GPIO118	TRIG0	SWO	CT118	NCE118	UART1_TX	UART0_CTS	I2S0_CLK	-	X		2
119	-	-	BTDM_RXEN	GPIO119	TRIG1	SWO	CT119	NCE119	UART1_RX	UART0_RTS	ST_WCI_2W_RXD	-	X		5

Table 18: Pad Function Color Code

Color/Symbol	Module
Analog	Analog Modules (ADC, VCOMP)
BTDM	BTDM
CLKOUT	Clock Output
COEX/ST_WCI	Wireless Coexistence
CT	Counter/Timer
DBIB	MIPI DBI Type B Display Interface
Debug	Debug/Special
DISP	Display Interface
GPIO	General Purpose Input/Output
I2S0	Inter-IC Sound 0
IOM0	I2C/SPI Manager 0
IOM1	I2C/SPI Manager 1
IOM2	I2C/SPI Manager 2
IOM3	I2C/SPI Manager 3
IOM4	I2C/SPI Manager 4
IOM5	I2C/SPI Manager 5
IOS	I2C/SPI Subordinate
MSPI0	Multi-bit Serial Peripheral Interface 0
MSPI1	Multi-bit Serial Peripheral Interface 1
MSPI2	Multi-bit Serial Peripheral Interface 2
NCE/MNCE	IOM/MSPI Chip Enables
PDM0	PDM-to-PCM Converter
PDMI2S0	PDMI2S0
SDIF0	Secure Digital Input Output Interface 0
SDIF1	Secure Digital Input Output Interface 1
UART0	Universal Asynchronous Receiver/Transmitter 0
UART1	Universal Asynchronous Receiver/Transmitter 1
USB	Universal Serial Bus

13.5 Additional Information

Please refer to the GPIO registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

14. General Purpose ADC and Temperature Sensor Module

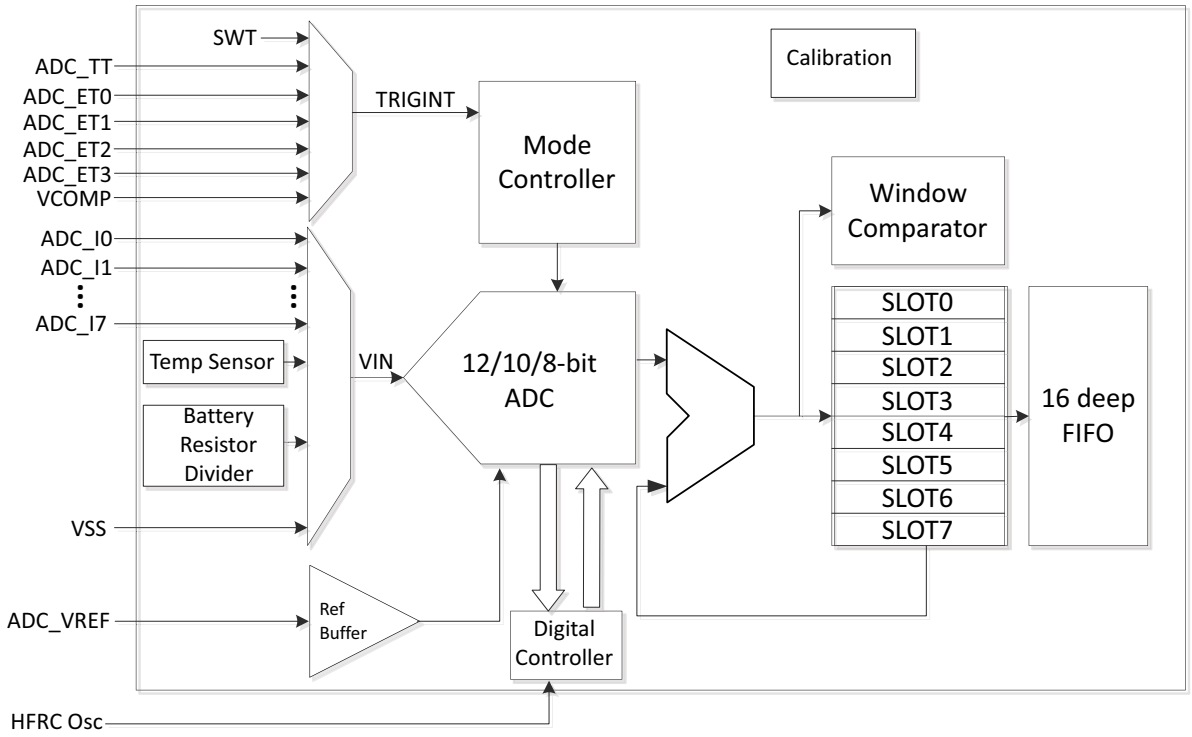

Figure 18. Block Diagram for ADC and Temperature Sensor

14.1 Features

The general purpose Analog-to-Digital Converter (ADC) and Temperature Sensor Module include a single-ended 12-bit multichannel Successive Approximation Register (SAR) ADC as shown in Figure 18.

Key features include:

- 11 user-selectable channels with sources including:
  - 8 single ended external pins
  - Internal voltage (VSS)
  - Voltage divider (battery)
  - Temperature sensor with ±3ºC accuracy
- Configurable automatic low power control between scans
- Optional battery load enable for voltage divider measurement
- Single shot, repeating single shot, scan, and repeating scan modes
- Variable sample tracking time, configurable on per-slot basis
- User-selectable clock source for variable sampling rates
- Automatically accumulate and scale module for hardware averaging of samples
- A 16-entry FIFO and DMA capability for storing measurement results and maximizing MCU sleep time
- Supports ping-pong DMA jobs
- Window comparator for monitoring excursions of voltage into or out of user-selectable thresholds
- Up to 2.8 MS/s effective continuous, multi-slot sampling rate (at 8-bit resolution)
- Interrupts for FIFO full, FIFO 75% full, Scan Complete, Conversion Complete, Window Incursion, Window Excursion, and various DMA-related notifications

14.2 Functional Overview

The Apollo510 Lite SoC integrates a 12-bit successive approximation Analog to Digital Converter (ADC) block for sensing both internal and external voltages. The block provides eight separately managed conversion requests, called slots which are serially sequenced. The result of each conversion requests is delivered to a 16 deep FIFO. Firmware can utilize various interrupt notifications to determine when to collect the sampled data from the FIFO or from a buffer written by DMA. This block is extremely effective at automatically managing its power states and its clock sources.

The ADC supports one internal reference source used for the analog to digital conversion step. The reference voltage, V_{ADCREF}, is as specified in the Electricals section (Table 46, “Analog-to-Digital Converter (ADC),” on page 222) and is not user settable. ADC input voltages > V_{ADCREF} exceed the ADC range and return full scale code, but will not damage ADC inputs.

DMA jobs may be ping-pong processed to allow software to pre-process and/or post-process one DMA job while hardware is processing another DMA job.

14.3 Voltage Divider and Switchable Battery Load

The Apollo510 Lite SoC’s ADC includes a switchable voltage divider that enables the ADC to measure the input voltage to the VDD rail. In most systems this will be the battery voltage applied to the SoC. The voltage divider is only switched on when one of the active slots is selecting analog mux channel 9. That is only when the mode controller is ultimately triggered and powers up the ADC block for a conversion scan of all active slots. Otherwise, the voltage divider is turned off.

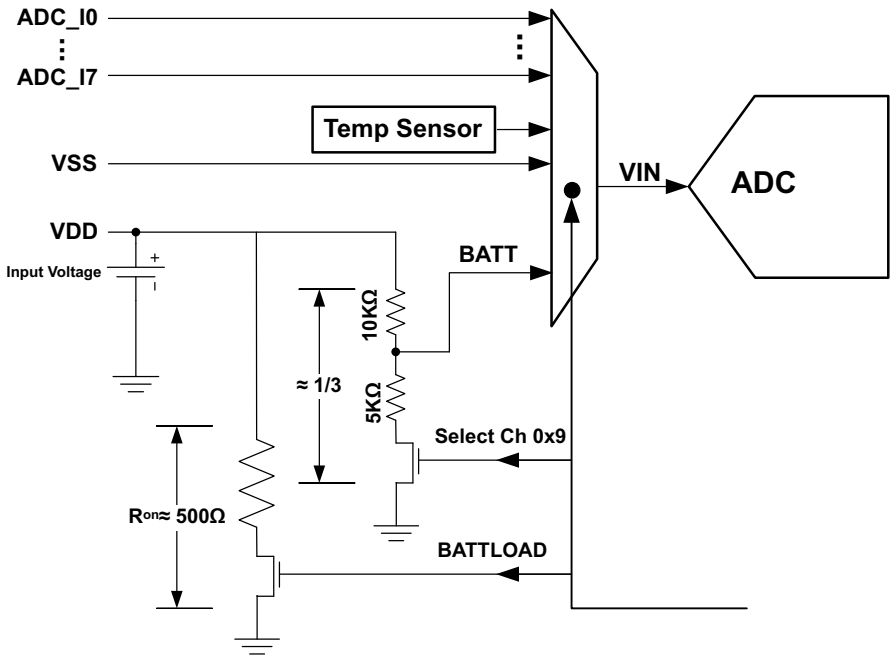

Figure 19. Switchable Battery Load

The switchable load resistor is enabled by the BATTLOAD bit as shown in the ADCBATTLOAD Register of the MCUCTRL Registers.This feature is used to help estimate the health of the battery chemistry by estimating the internal resistance of the battery.

14.4 Additional Information

Please refer to the ADC registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

15. Voltage Comparator (VCOMP)

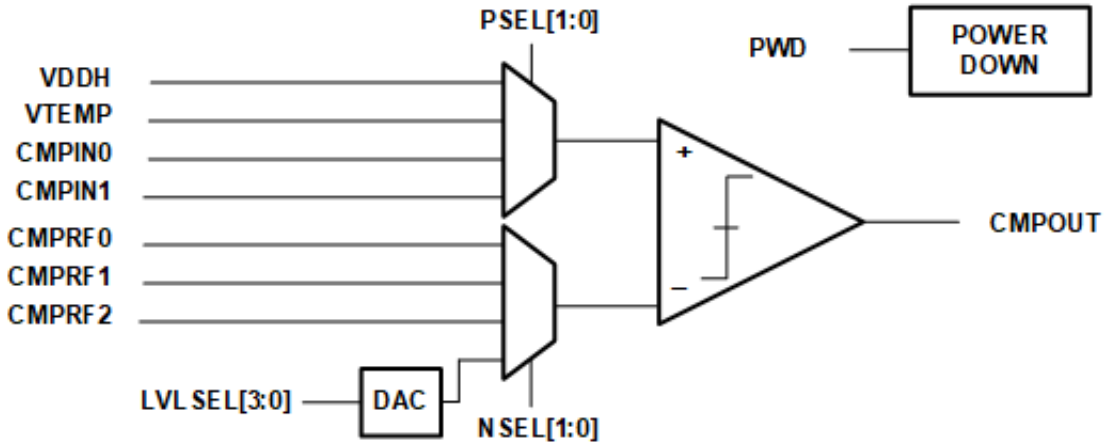

Figure 20. Voltage Comparator Block Diagram

15.1 Features

The Voltage Comparator (VCOMP) includes features shown in Figure 20 and listed below.

- Measures a user-selectable voltage
- Multiple options for input and reference voltages
- Provides interrupt and software access to comparator output
- Can generate an interrupt when monitored voltage rises above or drops below a user-configurable threshold
- Monitored voltage may be any of:
  - Supply voltage (VDDH)
  - The PTAT voltage from the temperature sensor (VTEMP)
  - One of two external voltage channels - CMPIN0, CMPIN1
- Reference voltage may be any of:
  - Three external voltage channels - CMPRF0, CMPRF1, CMPRF2
  - Internally generated reference voltage (VREFINT) tunable using on-chip DAC with level select signal LVLSEL[3:0].
- VCOMPOUT output remains high while the positive input is above reference input and transitions low when the positive input falls below the reference input
- CMPOUT output directly accessible via register read
- Two settable interrupts
  - OUTHI can trigger if VCOMPOUT transitions high
  - OUTLOW can trigger if VCOMPOUT transitions low

15.2 Functional Overview

The Voltage Comparator Module in the Apollo510 Lite SoC measures a user-selectable voltage at all times. It provides interrupt and software access to the comparator output with multiple options for input and reference voltages. It can be configured to generate an interrupt when the monitored voltage rises above a user-configurable threshold or when the monitored voltage drops below a user-configurable threshold.

The voltage to be monitored is selected by programming the comparator's positive terminal signal, CFG_PSEL[1:0] and may be any of:

1. The supply voltage (VDDH)

2. The PTAT voltage from the temperature sensor (VTEMP)
3. Two external voltage channels selected by a GPIO function (CMPIN0 and CMPIN1)

The reference voltage is selected by programming the comparator's negative terminal, CFG_NSEL[1:0] and may be either of:

1. Three external voltage channels selected by a GPIO function (CMPRF0, CMPRF1, CMPRF2)
2. The internally generated reference voltage selected by CFG_LVLSEL

The internal reference voltage is tuned using an on-chip DAC with level select signal LVLSEL[3:0]. When using external inputs or reference inputs, the associated pads must be configured using the GPIO function selects explained in the GPIO document section.

The Voltage Comparator CMPOUT output will remain high while the voltage at the positive input is above the voltage at reference input. The CMPOUT output will transition low when the voltage at the positive input to the comparator falls below the reference input taking into account hysteresis. The CMPOUT output is directly accessible by software by reading the CMPOUT field in the status register. The OUTHI interrupt will be set if enabled and the CMPOUT transitions high or if it is high at the time the interrupt is enabled. Similarly, the OUTLOW interrupt will be set if enabled and the CMPOUT output transitions low or if it is low at the time the interrupt is enabled.

15.3 Additional Information

Please refer to the VCOMP registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

16. Multi-bit Serial Peripheral Interface (MSPI)

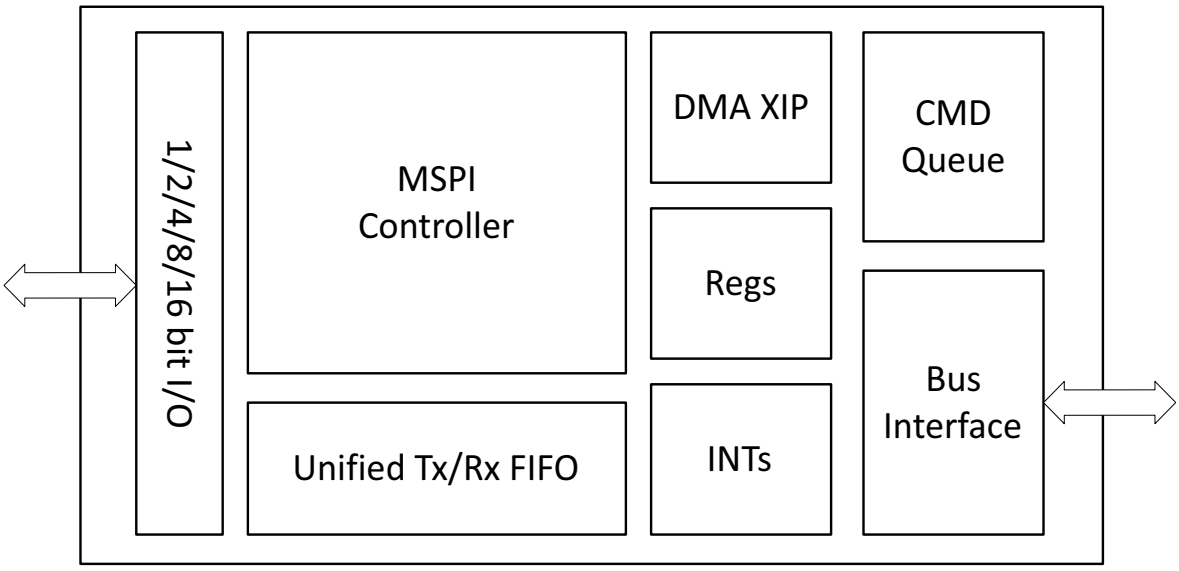

Figure 21. MSPI Module Block Diagram

16.1 Features

Each of the Multi-bit Serial Peripheral Interface (MSPI) modules includes the major functional blocks as shown in Figure 21.

Key MSPI features include:

- 1x HexSPI controller
  - 1/2/4/8/16-bit SPI interface
  - SDR/DDR modes
  - Up to 125 MT/s SDR and 250 MT/s DDR throughput on MSPI0
  - Supports up to 256 MB devices on MSPI0
  - Interoperability with JESD-251 rev C-compliant devices
- 1x OctalSPI controller
  - 1/2/4/8-bit SPI interface
  - SDR/DDR modes
  - Up to 125 MT/s SDR and 250 MT/s DDR throughput on MSPI2
  - Supports up to 64 MB devices
- 1x QuadSPI controller
  - 1/2/4-bit SPI interface
  - SDR/DDR modes
  - Up to 48 MT/s SDR and 96 MT/s DDR throughput on MSPI1
  - Supports up to 64 MB devices
- 9-bit command mode support
- XiP support
- Concurrent dual device support
- DMA with peripheral-to-memory and peripheral-to-peripheral support
- Command Queue support
- All four SPI CPOL/CPHA modes supported

NOTE

MSPI1 is not pinned out on the WLCSP package of Apollo510 Lite SoC. Also, MSPI2 supports up to QuadSPI data width on the WLCSP package.

NOTE

There is no full-duplex operation in 4-wire SPI mode of an MSPI on the Apollo510 Lite SoC. As well, MSPI 4-wire mode does not support reads of an arbitrary length, instead it always reads multiples of 4.

Please refer to the MSPI registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

16.2 Functional Overview

The Apollo510 Lite SoC includes three Multi-bit SPI (MSPI) modules which can be used to connect to external memory mapped devices. Each of the three MSPI modules supports data widths and clock/transfer rates as follows:

- MSPI0 can transfer in serial, dual, quad, octal and hex modes and supports operation up to 125 MHz DDR (250 MT/s).
- MSPI1 can transfer in serial, dual and quad modes and supports operation up to 48 MHz DDR (96 MT/s).
- MSPI2 can transfer in serial, dual, quad and octal modes and supports operation up to 125 MHz DDR (250 MT/s). A second set of (shared) quad mode MSPI2 pins offered for when MSPI0 is in hex mode (BGA package only), supports operation up to 24 MHz DDR (48 MT/s).

With these supported interface widths for the MSPIs pinned out on the BGA and WLCSP packages, the following configurations are possible:

- BGA
    1. 1x Hex SPI at 125 MHz / 250 MT/s (MSPI0), 1x QSPI at 48 MHz / 96 MT/s (MSPI1), 1x QSPI at 24 MHz / 48 MT/s (MSPI2's slower pins)
    2. 2x Octal SPI at 125 MHz / 250 MT/s (MSPI0, MSPI2), 1x QSPI at 48 MHz / 96 MT/s (MSPI1)

- WLCSP
    1. 1x Hex SPI at 125 MHz / 250 MT/s (MSPI0)
    2. 1x Octal SPI at 125 MHz / 250 MT/s (MSPI0), 1x Quad SPI at 125 MHz / 250 MT/s (MSPI2)

Each MSPI module has a unified 32-entry FIFO (32 bits wide) that is used for both transmit and receive data. To ensure that transactions are not dropped because of system or software latency, the MSPI controller pauses the clock (and thus the transfer on the bus) if the TX FIFO empties or the RX FIFO fills during an operation. It automatically resumes once the FIFO condition has cleared.

MSPI transfers generally consist of transmitting a 1-byte instruction, a 1-byte to 4-byte address (optional), and 1 byte to 16 MB of write or read data (with an optional number of turnaround clock cycles between address0 and RX data, as well as an optional number of turnaround clock cycles between address and RX data).

Most devices use the same number of pins to transmit instruction, address, and data (for example, all are quad or all are serial). However, some devices utilize mixed transfer modes to implement parallel data transfer on top of an inherently serial command structure. These devices are supported by the MSPI by utilizing the XIPMIXEDn configuration, which forces the MSPI to switch into dual or quad modes of operation for a portion of the transfer.

To utilize mixed mode transfers, the MSPI's normal configuration should be set to match the device's transfer characteristics for commands (usually serial), which allows the MSPI to communicate with the device in its native mode. The XIPMIXEDn field in the DEVnXIP register should then be programmed to indicate whether the data phase (and optionally address phase) of the command should be performed in dual or quad mode. The MSPI will automatically switch to the new mode after transmitting the command to the device for all DMA and XIP operations.

The MSPIn modules of the Apollo510 Lite SoC are directly attached to the system AXI bus and are memory mapped. For example, data read/write accesses and instruction accesses (referred to as XIP for eXecute In Place) for MSPI0 are via the 0x60000000 - 0x6FFFFFFF (non-secure) address range. Each MSPIn device register space has provisions to support two independent devices, however this is not currently supported in the Apollo510 Lite SoC. Only the DEV0* registers which configure the first device are valid. The device selected for the transaction can be specified in the PIODEV field (for PIO operations), DMADEV field (for DMA operations), or by the address range for memory-mapped operations. Each MSPIn device supports the configuration of two external devices which can be mapped within the MSPIn's memory region using the DEVnAXI configuration registers.

The MSPI modules of the Apollo510 Lite SoC are memory mapped as follow:

- MSPI0: 0x60000000 - 0x6FFFFFFF
- MSPI1: 0x80000000 - 0x83FFFFFF
- MSPI2: 0x84000000 - 0x87FFFFFF

NOTE
MSPI1 is not pinned out on the WLCSP package of Apollo510 Lite SoC.

Access to the MSPI devices is as follows:

- Cortex-M55 instruction accesses to XIP space are read-only and handled through the Cortex-M55 I-cache (which must be enabled).
- Cortex-M55 data accesses to XIP space are read/write and handled through the Cortex-M55 D-cache (which must be enabled). The GFX and the display controller access data directly through the XIP interface.
- PIO: The SoC can initiate PIO-based operations to manage basic device configuration and other low-level manual operations.
- DMA: MSPI module can autonomously transfer data between the external device and internal memory or NVM.

Note that XIP and DMA do not enforce hardware coherency, so the cache must be managed by software when performing DMA or XIP operations to regions that contain code which may be cached. In each of these modes, the MSPI module also supports data scrambling on accesses within a programmable address range having boundaries aligned to 64 kB address boundaries. Once the external devices are configured, the MSPI supports a simple DMA model, where software can program the internal (SRAM or flash) address and external device address, transfer direction, and transfer size. Once enabled, the MSPI DMA interface will move data between the system and external flash and interrupt when complete. The MSPI also supports a higher-level command queuing (CQ) protocol, where software can construct a buffer of operations in SRAM (or internal flash memory) and the MSPI will execute the series of operations autonomously. The MSPI can also power itself down at the end of DMA or CQ operations.

While each MSPI module can be used as a generic SPI device (with two chip enables), in addition to supporting serial, dual, and quad displays, it is primarily designed to support serial NAND/NOR flash memory or PSRAM memory. It is intended to be used to initialize the external memory devices and then be configured with the parameters matching the flash access characteristics. Devices can then be accessed through DMA or XIP operations with minimal software overhead.

The DMA address range has been expanded to support the larger flash and SRAM sizes, and the MSPI DMA/transfer length has been expanded to 24 bits to allow burst transactions of more than 64 kB.

The MSPI module also contains:

- A DEVnBOUNDARYn register which can be programmed to break a single long MSPI DMA into smaller transfers at periodic intervals (DMATIMELIMITn bit field).
- Address boundaries (DMABOUNDn bit field) to provide breaks in DMA for XIP traffic and satisfy the page crossing and maximum refresh times of external PSRAM devices.

NOTE

The DMATIMELIMITn is approximate since the MSPI will continue transmitting to the next 32-bit word boundary before disengaging on the bus. For this reason, a device requiring an 8 µs maximum transmission time should be set to have about a 7.5 µs time limit.

NOTE

For DMABOUNDn to properly break at a page crossing, the DMADEVADDR for the transfer must be 4-byte aligned. If a non-aligned starting edge of the transfer is required, software should manually break the transaction into two parts, with the first transaction ending on the page boundary. Failure to observe this limitation will result in data loss as the MSPIn may write 1-3 additional bytes past the boundary which will either wrap within the device's page or be discarded by the device.

16.2.1 Configuring MSPI as a DMA Target and a DMA Client Concurrently

A DMA deadlock may occur when there is heavy traffic of concurrent DMA accesses such as when the MSPI is used as both a “DMA client”, where MSPI is sourcing or sinking data through the DMA, and a “DMA target”, where MSPI is a memory-mapped source or destination for other peripheral DMA. For example, a situation may exist when the ADC is targeting a memory device through the MSPI XIPMM aperture as a the ADC sample “DMA target” at the same time that the MSPI is using DMA itself to target SSRAM or TCM. This condition may result in a DMA deadlock due to a circular dependency when the APBDMA-AXI, MSPI-AXI, MSPI-XIPDMA and APBDMA-ARBITOR states are blocking or waiting for DMA resources.

To avoid this potential problem, software should control the DMA’s configuration to alternate between MSPI as a DMA client and as a DMA target so as not to allow overlap of these DMA accesses. Note that there should not be a threat of this deadlock situation when short CPU accesses such as XIP or memory mapped MSPI are occurring, due to the location of arbitration against DMA traffic.

16.3 Pad Configuration and Enables

For the Apollo510 Lite SoC all three MSPI modules, MSPI0-MSPI2, support serial, dual or quad mode, while MSPI2 additionally supports octal mode and MSPI0 additionally supports octal or hex mode. Each MSPI module supports the external connections shown in the following tables. The columns to the right indicate which bits are used in each configuration (S=serial, D=dual, Q=quad, O=octal with CE#). Within the table, O=output pin, I=input pin, and X=bidirectional.

NOTE

MSPI1 is not pinned out on the WLCSP package of Apollo510 Lite SoC.

NOTE

Maximum clock speed of a specific SPI interface is dependent on the timing characterization of the chip enable (CEn) for each MSPI instance. Those speeds are specified in the Electricals chapter.

Table 19: MSPI0 Pin Muxing (Serial, Dual, Quad, Octal, Hex)

Pin Name	Direction	GPIO	Description	S0	S1	D0	D1	Q0	Q1	O0	O1	H0	H1
MSPI0.0	Output	78*	MSPI0 CE0	O		O		O		O		O	
MSPI0.1	Output	79	MSPI0 CE1		O		O		O		O		O
MSPI0_18	Input/Output	77	MSPI0 DM1/DQS1 (Hex)									X	X
MSPI0_17	Input/Output	76	MSPI0 Data Bit 15									X	X
MSPI0_16	Input/Output	75	MSPI0 Data Bit 14									X	X
MSPI0_15	Input/Output	74	MSPI0 Data Bit 13									X	X
MSPI0_14	Input/Output	73	MSPI0 Data Bit 12									X	X
MSPI0_13	Input/Output	72	MSPI0 Data Bit 11									X	X
MSPI0_12	Input/Output	71	MSPI0 Data Bit 10									X	X
MSPI0_11	Input/Output	70	MSPI0 Data Bit 9									X	X
MSPI0_10	Input/Output	69	MSPI0 Data Bit 8									X	X
MSPI0_9	Input/Output	81	MSPI0 DM0/DQS0 (Octal/Hex)							X	X	X	X
MSPI0_8	Output	35	MSPI0 CLK	O	O	O	O	O	O	O	O	O	O
MSPI0_7	Input/Output	68	MSPI0 Data Bit 7							X	X	X	X
MSPI0_6	Input/Output	67	MSPI0 Data Bit 6							X	X	X	X
MSPI0_5	Input/Output	66	MSPI0 Data Bit 5							X	X	X	X
MSPI0_4	Input/Output	65	MSPI0 Data Bit 4							X	X	X	X
MSPI0_3	Input/Output	39	MSPI0 Data Bit 3					X	X	X	X	X	X
MSPI0_2	Input/Output	38	MSPI0 Data Bit 2					X	X	X	X	X	X
MSPI0_1	Input/Output	37	MSPI0 Data Bit 1	I	I	X	X	X	X	X	X	X	X
MSPI0_0	Input/Output	36	MSPI0 Data Bit 0	O	O	X	X	X	X	X	X	X	X

*Not pinned out on the WLCSP package

Table 20: MSPI1 Pin Muxing (Serial, Dual, Quad)

Pin Name	Direction	GPIO	Description	S0	S1	D0	D1	Q0	Q1
MSPI1.0	Output	40	MSPI1 CE0	O		O		O	
MSPI1.1	Output	42	MSPI1 CE1		O		O		O
MSPI1_5	Input/Output	52	MSPI1 DM/DQS					X	X
MSPI1_4	Output	47	MSPI1 CLK	O	O	O	O	O	O
MSPI1_3	Input/Output	51	MSPI1 Data Bit 3					X	X
MSPI1_2	Input/Output	50	MSPI1 Data Bit 2					X	X
MSPI1_1	Input/Output	49	MSPI1 Data Bit 1	I	I	X	X	X	X
MSPI1_0	Input/Output	48	MSPI1 Data Bit 0	O	O	X	X	X	X

NOTE
MSPI1 is not pinned out on the WLCSP package of Apollo510 Lite SoC.

Table 21: MSPI2 Pin Muxing (Serial, Dual, Quad, Octal)

Pin Name	Direction	GPIO	Description	S0	S1	D0	D1	Q0	Q1	O0	O1
MSPI2.0	Output	41*, 110	MSPI2 CE0	O		O		O		O	
MSPI2.1	Output	80*, 111*	MSPI2 CE1		O		O		O		O
MSPI2_9	Input/Output	58*, 77	MSPI2 DM0/DQS0 (Octal)							X	X
MSPI2_8	Output	53*, 112*	MSPI2 CLK	O	O	O	O	O	O	O	O
MSPI2_7	Input/Output	76	MSPI2 Data Bit 7							X	X
MSPI2_6	Input/Output	75	MSPI2 Data Bit 6							X	X
MSPI2_5	Input/Output	74	MSPI2 Data Bit 5							X	X
MSPI2_4	Input/Output	73	MSPI2 Data Bit 4							X	X
MSPI2_3	Input/Output	57*, 72	MSPI2 Data Bit 3					X	X	X	X
MSPI2_2	Input/Output	56*, 71	MSPI2 Data Bit 2					X	X	X	X
MSPI2_1	Input/Output	55*, 70	MSPI2 Data Bit 1	I	I	X	X	X	X	X	X
MSPI2_0	Input/Output	54*, 69	MSPI2 Data Bit 0	O	O	X	X	X	X	X	X

*Not pinned out on the WLCSP package (MSPI2 Clk must be set to MSPI2_4, eliminating the use of Octal data width for MSPI2).

The PADOUTEN register should be programmed to enable the proper pins for the selected mode. If using any mode with a data width less than Octal, the output clock can selectively be switched from the standard clock pin, MSPIn_8, to data bit 4 by setting the CLKOND4 bit[1]. Typically, most serial SPI devices use a separate MOSI and MISO when operating in serial mode. The SEPIO0 or SEPIO1 bits in the DEV0CFG or DEV1CFG registers, respectively, should be set when software needs to read data from devices in serial mode, since it redirects the MISO input from pin 1 down to input data pin 0 of the MSPI's RX logic.

Table 22 below shows the required field configurations for typical MSPI operating modes. It should be noted that if the PADOUTEN_CLKOND4 is set to move the CLK pin from MSPIn_8 to MSPIn_4 (serial, dual or quad mode), then the PADOUTEN_OUTEN field must be adjusted accordingly, e.g., 0x101 becomes 0x011.

The I/O widths for data, address and instruction phases do not need to be the same in either PIO mode or XIP/DMA mode. 1-4-4 and other such mixed modes refer to the width of the instruction, address and data phases of the MSPI bus, respectively. The width(s) of the data phase, or both the address and data phases, of a PIO command are selected by the PIOMIXED field of the MSPI_CTRL1 register where device0 or device1 is selected by the PIODEV field of the MSPI_CTRL register or, for a XIP transaction, by the XIPMIXEDn field of the MSPI_DEVnXIP register where n is device0 or device1 for the particular MSPI

1. Note that on MSPI1, there is no MSPI1_8 pin and therefore CLKOND4 must be used and set for the clock line.

instance. Depending on the I/O widths supported by the MSPI instance, the data width or both data and address widths can be specified as dual, quad or octal width.

Table 22: Required Settings for Typical MSPI Configurations

Mode (Data Lines and CE)					DEV0CFG_ DEVCFG0	DEV0CFG_ SEPIO0	DEV0XIP_ XIPMIXED0	PADOUTEN_ OUTEN
Instruction	Address	Data	Separate IO	Chip Enable (CE)				
Serial	Serial	Serial	Yes	0	SERIAL0 (1)	1	NORMAL (0)	SERIAL0 (0x103)
Serial	Serial	Serial	Yes	1	SERIAL1 (2)	1	NORMAL (0)	SERIAL0 (0x103)
Serial	Serial	Serial	No	0	SERIAL0 (1)	0	NORMAL (0)	0x101
Serial	Serial	Serial	No	1	SERIAL1 (2)	0	NORMAL (0)	0x101
Serial	Serial	Dual	No	0	SERIAL0 (1)	0	D2 (1)	SERIAL0 (0x103)
Serial	Serial	Dual	No	1	SERIAL1 (2)	0	D2 (1)	SERIAL0 (0x103)
Serial	Dual	Dual	No	0	SERIAL0 (1)	0	AD2 (3)	SERIAL0 (0x103)
Serial	Dual	Dual	No	1	SERIAL1 (2)	0	AD2 (3)	SERIAL0 (0x103)
Serial	Serial	Quad	No	0	SERIAL0 (1)	0	D4 (5)	QUAD0 (0x10F)
Serial	Serial	Quad	No	1	SERIAL1 (2)	0	D4 (5)	QUAD0 (0x10F)
Serial	Quad	Quad	No	0	SERIAL0 (1)	0	AD4 (7)	QUAD0 (0x10F)
Serial	Quad	Quad	No	1	SERIAL1 (2)	0	AD4 (7)	QUAD0 (0x10F)
Dual	Dual	Dual	No	0	DUAL0 (5)	0	NORMAL (0)	SERIAL0 (0x103)
Dual	Dual	Dual	No	1	DUAL1 (6)	0	NORMAL (0)	SERIAL0 (0x103)
Quad	Quad	Quad	No	0	QUAD0 (9)	0	NORMAL (0)	QUAD0 (0x10F)
Quad	Quad	Quad	No	1	QUAD1 (0xA)	0	NORMAL (0)	QUAD0 (0x10F)
Octal	Octal	Octal	No	0	OCTAL0 (0xD)	0	NORMAL (0)	OCTAL (0x3FF)
Octal	Octal	Octal	No	1	OCTAL1 (0xE)	0	NORMAL (0)	OCTAL (0x3FF)
Hex	Hex	Hex	No	0	HEX0 (0x11)	0	NORMAL (0)	HEX (0x7FFFF)
Hex	Hex	Hex	No	1	HEX1 (0x12)	0	NORMAL (0)	HEX (0x7FFFF)

16.4 Board/Package Considerations for MSPI Pin Timing

16.4.1 Delay Step Size

Each delay step discussed in this section represents a delay of 80 to 200 ps / LSB per the DDR Delay Step Size provided in the MSPI section of the Electrical Characteristics.

16.4.2 SDR Mode with non-DQS

The timing parameters specified in the datasheet are based on 0-tap delay on both TX and RX delay lines, regardless of the actual number of taps being programmed. TX delay taps will delay the SCLK as illustrated by the red dotted line in Figure 22.

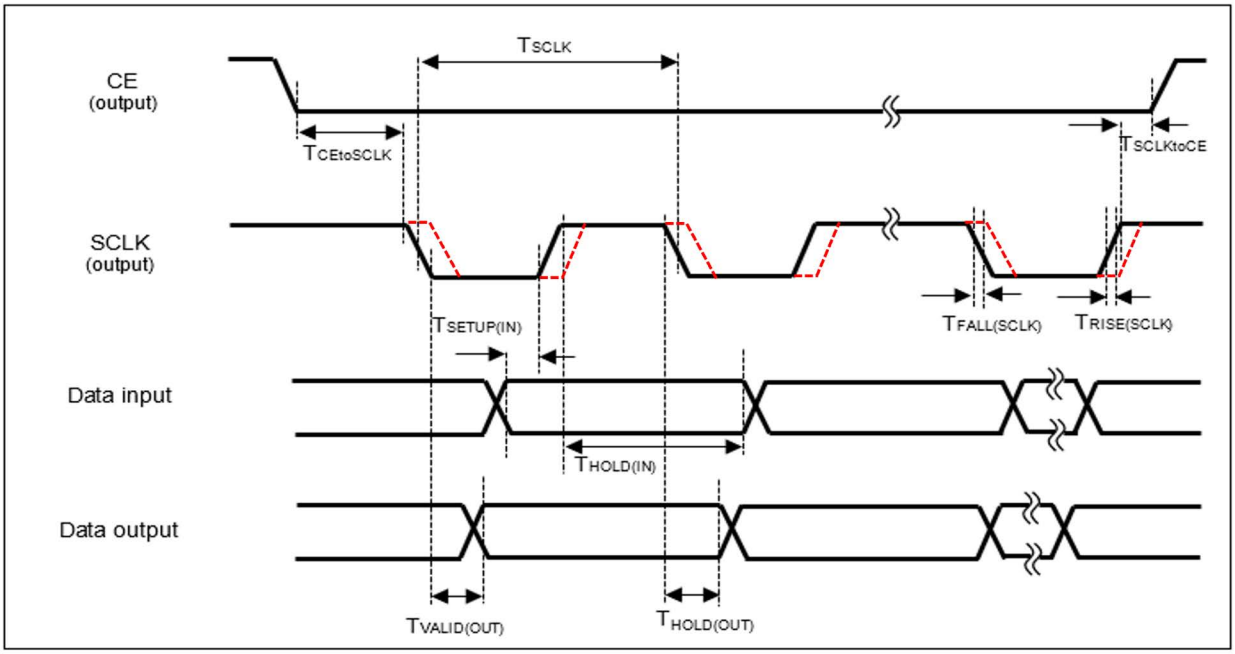

Figure 22. SDR Mode with Non-DQS

With more TX delay taps, Tvalid(out) will be sooner with respect to the delayed SCLK, but Thold(out) will be sooner as well.

The RX delay tap will delay the internal sampling clock (not shown in the timing diagram). With more RX delay taps, it allows a longer Tsetup(in) for external device, but a shorter Thold(in).

16.4.3 DDR Mode with DQS

The timing parameters specified in the MSPI section of the Electricals chapter are based on 0-tap delay on both TX and RX delay lines, regardless of the actual number of taps being programmed.

TX delay taps (TXDQSDELAY0) will delay the SCLK, as illustrated by the red dashed lines in the SCLK (output) waveform of Figure 23. With more TX delay taps, Tvalid(out) will be sooner with respect to the delayed SCLK, but Thold(out) will be sooner as well.

RX delay tap (RXDQSDELAY*0) will delay the DQS input in the chip, as illustrated by the red dashed lines in the DQS (input) waveform of Figure 23. With more RX delay taps, it allows a longer Tsetup(in) for external device, but a shorter Thold(in).

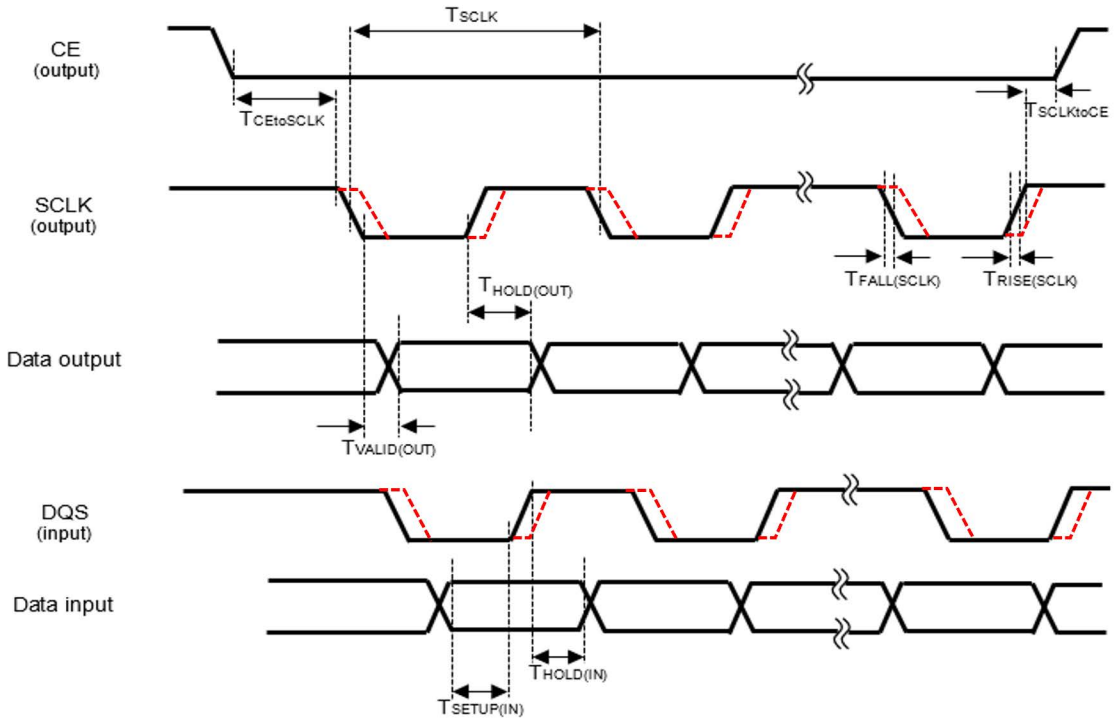

Figure 23. DDR Mode with DQS

Figure 24 shows DQS0 delay parameters in Octal/Hex DDR Mode with DQS, with respect to the input (RX) data byte (lower data byte for Hex) when RXDQSDELAYNEGEN = 0 and when RXDQSDELAYNEGEN = 1. See the fields in the DEVnDDR register which set these parameters.

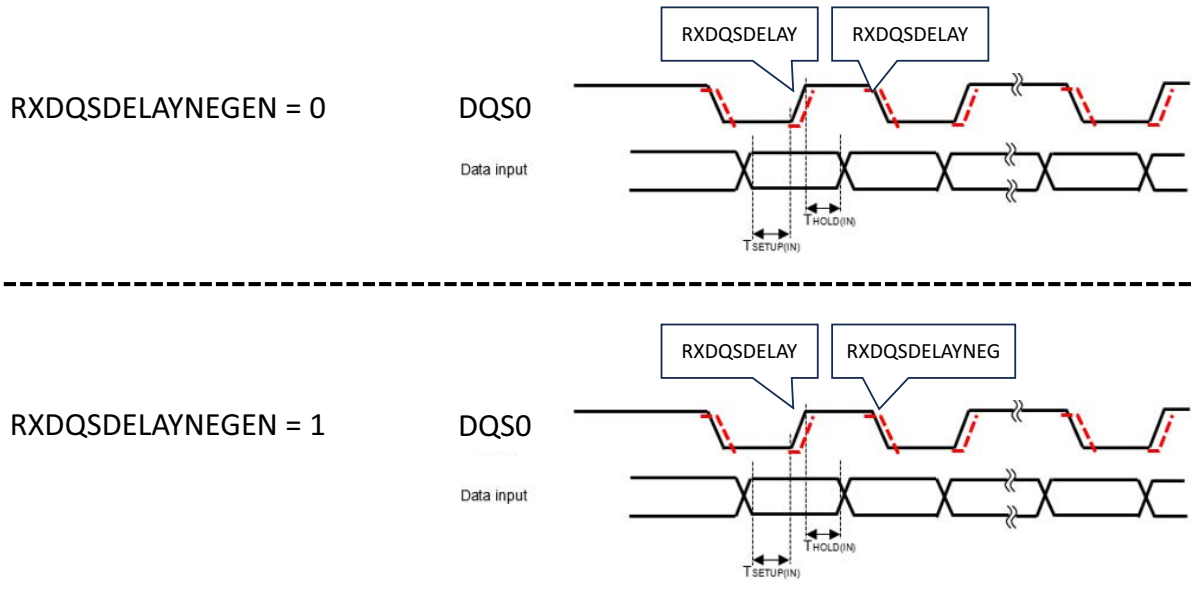

Figure 24. Octal/Hex DDR Mode with DQS - Read Delay Lines - Lower Data Byte DQS

Figure 25 shows DQS1 delay parameters in Hex DDR Mode with DQS, with respect to the upper input (RX) data byte under the following conditions:

1. RXDQSDELAYHIEN = 0 and RXDQSDELAYNEGEN = 0
2. RXDQSDELAYHIEN = 0 and RXDQSDELAYNEGEN = 1
3. RXDQSDELAYHIEN = 1 and RXDQSDELAYNEGEN = 0
4. RXDQSDELAYHIEN = 1 and RXDQSDELAYNEGEN = 1

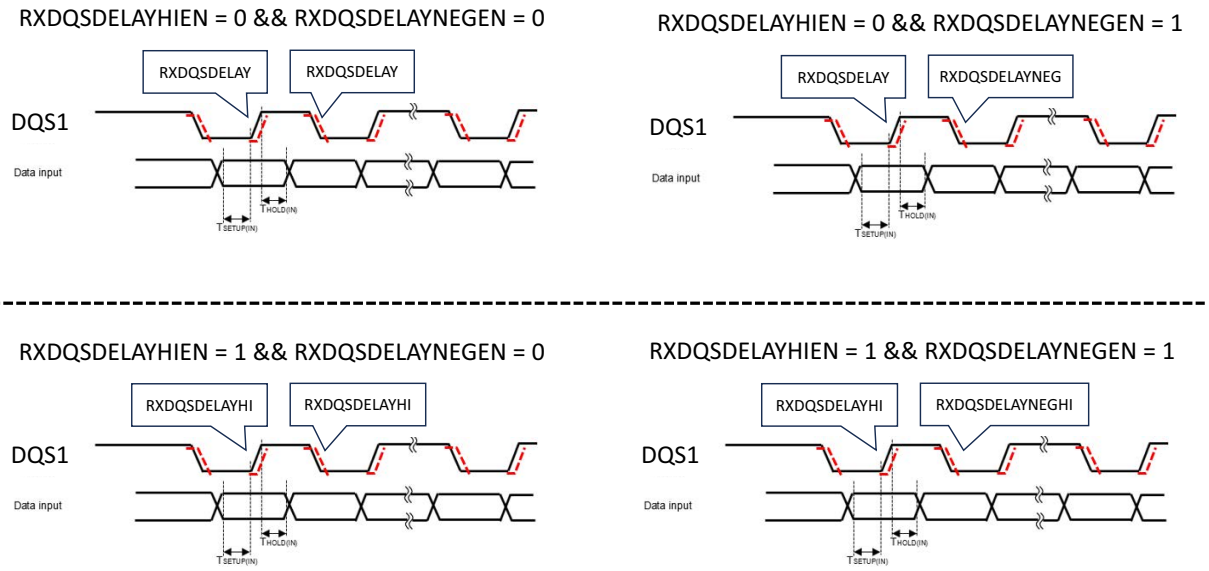

Figure 25. Hex DDR Mode with DQS - Read Delay Lines - Upper Data Byte DQS

16.5 Additional Information

Please refer to the MSPI registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

17. I²C/SPI Manager (IOM)

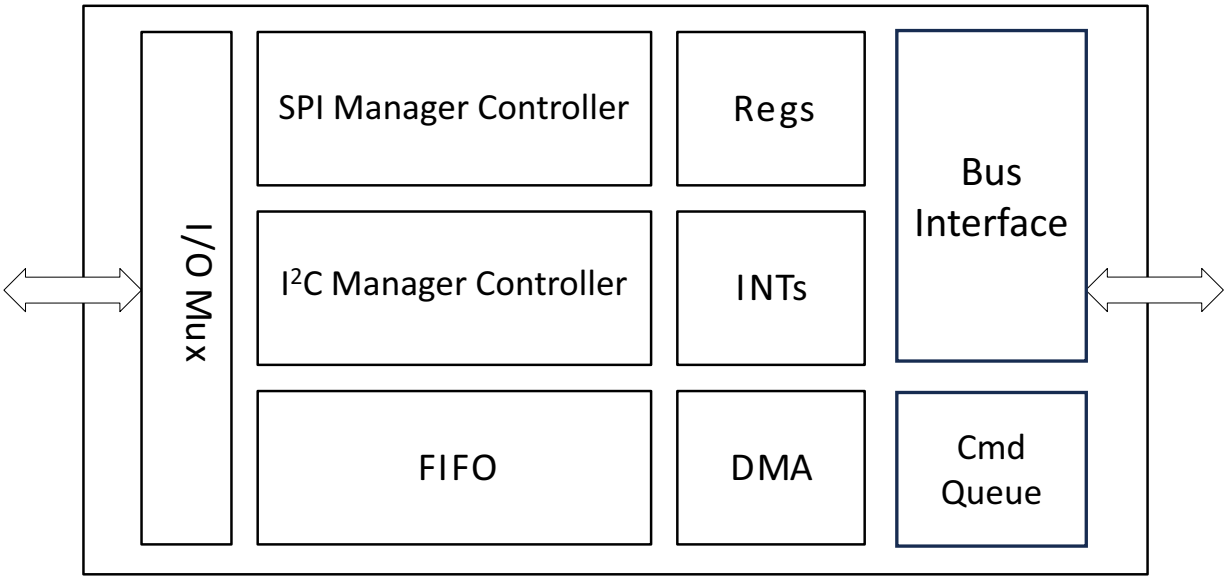

Figure 26. IOM Block Diagram

17.1 Features

The I²C/SPI Manager Module includes features shown in Figure 26 and listed below.

- Six (6) controller instances supporting up to 4 chip selects per instance
- Up to 24 MHz clock for SPI interface
- I²C and SPI modes
- DMA with peripheral-to-memory and peripheral-to-peripheral supported
- Command Queue support

NOTE
There is no full-duplex transfer operation for IOM DMA on the Apollo510 Lite SoC.

17.2 Functional Overview

The Apollo510 Lite SoC includes 6 I²C/SPI high-speed manager modules, each of which functions as the manager of an I²C or SPI interface as selected by the IOMm_SUBMODCTRL_SMODnEN bit (m = 0 to 5, n=0 or 1) register field. A 64-byte bidirectional FIFO and a sophisticated command mechanism allow simple initiation of I/O operations without requiring software interaction.

In I²C mode the I²C/SPI Manager supports 7- and 10-bit addressing, multi-manager arbitration, interface frequencies from 1.2 kHz to 1.0 MHz and up to 4095-byte burst operations. In SPI mode the I²C/SPI Manager supports up to 4 subordinates with automatic nCE selection, 3- and 4-wire implementation, all SPI polarity/phase combinations and up to 4095-byte burst operations, with both standard embedded

address operations and raw read/write transfers. Interface timing limits are as specified in the Serial Peripheral Interface (SPI) Manager Interface table of the Electrical Characteristics chapter.

NOTE

I^{2}C clock stretching operation is not guaranteed on this SoC. If an I^{2}C peripheral device that performs clock stretching is used, the recommendation is to perform compatibility testing with the Apollo510 I^{2}C interface.

17.3 Data Alignment

All data accesses between the MCU and the IOM interface are word aligned. Since the transfer size is specified in bytes, unused bytes within the word will either be discarded (for write operations) or filled with zero (read operations) to align to the next word boundary. DMA operations support a byte starting address, and the programmed DMA address does not have to be word aligned. Direct mode write operations will start transferring the least significant byte of the word (little endian style) at the current write FIFO pointer. If any remaining bytes are unused in a word at the end of the write operation, they will be discarded, and the write pointer will be set to the next word location. Direct mode read operations will store the first received byte into the least significant byte of location specified by the read FIFO pointer, and will fill any unused byte locations with zero if the transaction size is not a word multiple. The FIFO read pointer will point to the next FIFO location in the read FIFO, which will be word aligned.

17.3.1 Direct Mode Data Transfers

Direct mode data is enabled when DMA is disabled via the IOMn_DMACFG_DMAEN and the data transfer size (TSIZE) is greater than 0. In this mode, the MCU transfers data via direct writes or reads to registers in the IOM. The IOM maintains separate FIFO pointers for the read and write FIFOs, and updates these when a PUSH or POP register is accessed. Writing to the IOMn_FIFOPUSH register will perform a push event of the word into the FIFO and update the write pointer by 4 bytes. Only word accesses are supported to the IOM, and any unused bytes within a word will be discarded. An example of a 5 byte write transfer is shown below.

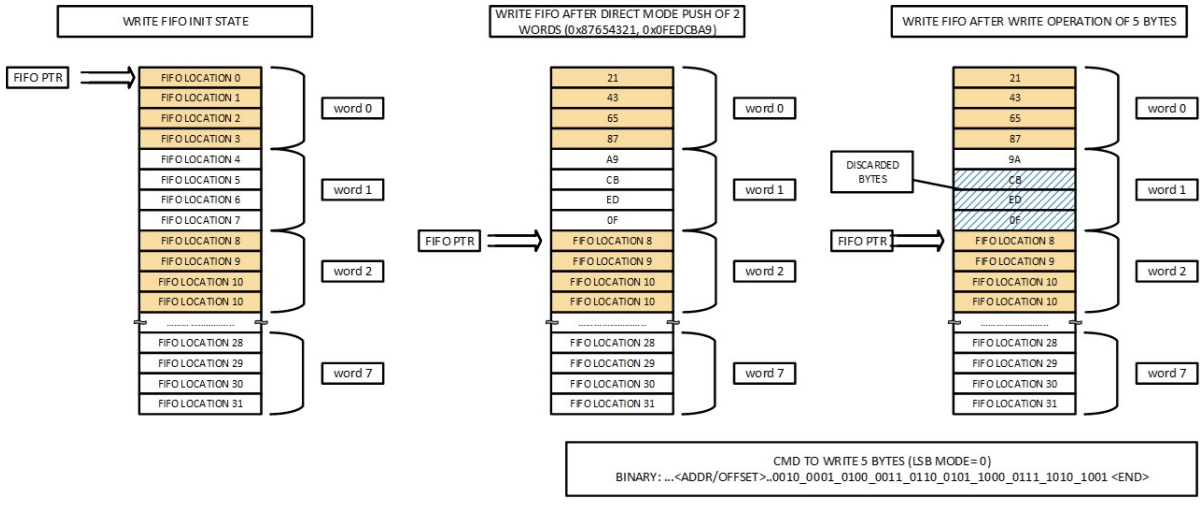

Figure 27. Direct Mode 5-byte Write Transfer

Reading from the IOMn_FIFOPOP register will perform a POP operation, return 4 bytes of data and advance the internal read FIFO pointer by 4 bytes. Any unused bytes within the read data will be filled with zeros and aligned to a word boundary at the end of the transaction. An example of a 5 byte read operation is shown below.

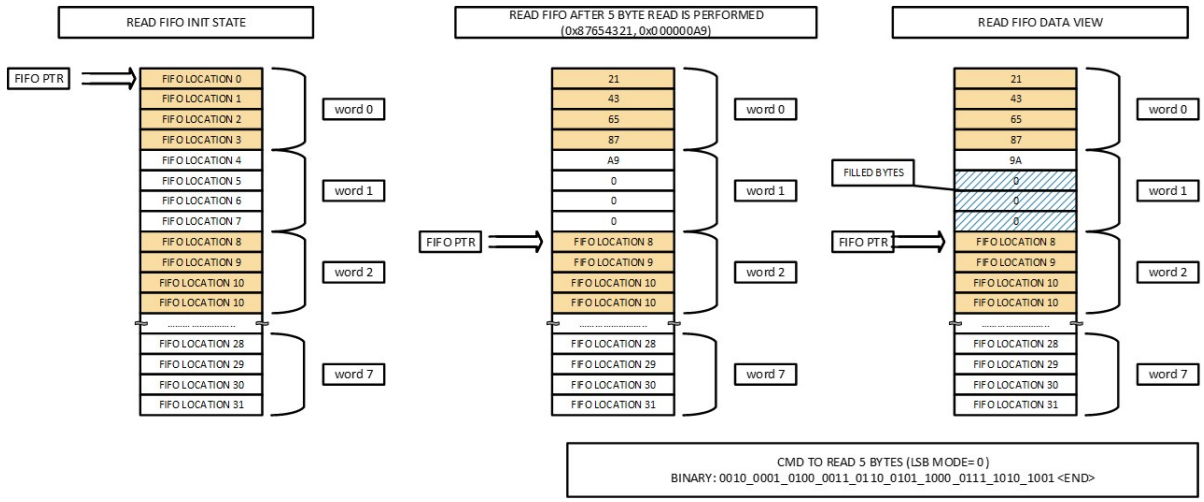

Figure 28. Direct Mode 5-byte Read

The IOM also supports a non-destructive POP mechanism to prevent unintended POP events from occurring. If the IOMn_FIFOCTRL_POPWR field is active (1), a write to the IOMn_FIFOPOP register will be required in order to complete the POP event. Reads will return the current data.

An active transaction will be paced by data availability and will hold the clock low if there is not enough data to continue write operations, or if the read FIFO is full during read operations. This wait condition is indicated when the IOMn_CMDSTAT_CMDSTAT field is 0x6. Once new data or FIFO locations are present, the command will continue operation automatically.

17.3.2 DMA Data transfers

DMA transfers are enabled by configuring the DMA related registers, enabling the DMA channel, and then issuing the command. The command will automatically fetch and store the data associated with the command without MCU intervention. The DMA channel is enabled via the IOMn_DMACFG_DMAEN field. P2M DMA operations transfer data from peripheral to memory and are used in IOM READ operations. M2P DMA operations transfer data from memory to peripheral and are used in IOM write operations. DMA transfer size is programmed into the IOMn_DMATOTCOUNT register and supports up to 4095 bytes of data transfer (over the SPI interface). The DMA transfer size is independent from the transaction size, and allows a single DMA setting to be used across multiple commands. The direction of DMA data transfer must match the command. The IOMn_DMACFG_DMAEN field enables/disables the DMA transfer capability and must be set last when configuring the DMA, generally prior to sending the command.

The DMA engine within the module will initiate a transfer of data when a trigger event occurs. There are 2 types of triggers available, threshold (THR) and command completion (CMDCMP). The THR trigger will activate when the threshold programmed into the FIFOWTHR or FIFORTHR in the IOMn_FIFOTHR register meets the data criteria. Because the MCU access to the interface is 32 bits wide, only the word count of the selected THR is used, and the low order bits of the FIFOWTHR or FIFORTHR are ignored.

During the transfer, the TOTCOUNT register is decremented to reflect the number of bytes transferred.

For IOM write operations (data written from IOM out to an external device), the THR trigger will activate when the write FIFO contains FIFOWTHR[5:2] free words. If the remaining DMA transfer size is less than this, only the needed number of words are transferred.

For IOM read operations (data read from external device), the THR trigger will activate when the read FIFO contains FIFORTHR[5:2] words of valid data. If the remaining DMA transfer size is less than the RTHR words, then the CMDCMP trigger can be enabled to transfer the remaining data. If the CMDCMP trigger is disabled, and the number of bytes in the read FIFO is greater to or equal to the current TOTCOUNT, a DMA transfer of TOTCOUNT will be done to complete the DMA operation. This mode requires that the THR trigger be enabled as well.

The CMDCMP trigger activates when the command is complete and will transfer the lesser of the TOTCOUNT or the number of bytes in the read FIFO. Note that this trigger is not needed for write operations, and the THR trigger should be used in this case. If a read operation is done, and the THR trigger is disabled, and only the CMDCMP trigger is enabled, and the transaction size is greater than the FIFO size (32 bytes), the module will hang, as there is no trigger to cause a DMA operation, and the logic will pause the interface until there is room within the read FIFO to store data.

If DMA transfer size is matched to the IOM transaction size, it is recommended to program both the FIFORTHR and FIFOWTHR to 0x10 (16 bytes) and only enable the THR trigger.

17.4 Transaction Initiation

To start a transaction, the IOM module must be powered up and the target external pins enabled via the GPIO module. For SPI transactions, this will generally require 4 pins to be enabled via the function select field of the PADREG registers in the GPIO module. The CEN pin for SPI transaction requires setting of the FNCSEL field of the appropriate pin, as well as the CFGREG of the corresponding pin. This also includes the setting of the default value of the CEN. This is needed to allow the IOM module to power down and not activate the CEN signal.

Once the IOM module is powered on, and the external pins configured, the IOM submodule must be enabled via the IOMn_SUBMODCTRL register. This will activate either the SPI or I^2C interface. Once this is complete, the submodule specific registers should be configured to set the desired mode and features. If DMA is desired, the DMA registers should also be set, with the IOMn_DMACTRL_DMAEN field set last. The registers relating to DMA operations are as follows:

- IOMn_DMATRIGEN – Sets the trigger source for starting a DMA transfer
- IOMn_DMACFG – Sets the DMA direction and enable for DMA
- IOMn_DMATOTCOUNT – Sets the total count of bytes to be transferred via the DMA operation. Recommended to match the IOMn_CMD.TSIZE field for simplicity.
- IOMn_DMATARGADDR – The source or destination address of the DMA data. Sources can be either SRAM or storage. Destination address can only be SRAM. This is the memory mapped address of the DMA data as accessed by the MCU.

After the module setup is complete, the command register is written. This will start the IO transfer. The IOMn_CMD register contains the command itself, along with other fields used in the command, such as channel number, offset counts and transfer size. The IOM supports 2 main commands, read and write. A read command will write user selectable number of offset bytes (0 to 3), and then read IOMn_CMD_TSIZE bytes, storing the data into the read FIFO. A write command will write the user selectable number of offset bytes (0 to 3), followed by a write of IOMn_CMD_TSIZE bytes sourced from the write FIFO. Transfer sizes can be 0-4095 bytes for SPI or I^2C operations. The number of offset bytes for each command is specified in the IOMn_CMD_OFFSETCNT field.

17.5 Command Queue

The IOM module can also fetch register write data from SRAM or storage, and update the registers as if the write was performed via the MCU. Register data is stored as a doublet of 2 words. The first word is the module register address offset, word aligned. The second word is the write data value. Once enabled, the command queue (CQ) will fetch the address and perform a write to the register. If no command is started by the register write, the next doublet will be fetched by the CQ. If a command is started (write to IOMn_CMD register is done), the CQ processing will wait until the transaction is complete before fetching the next register write doublet. This is shown in the diagram below. No prefetching is done via the CQ, and the register write operations are performed in series with the transactions. This allows a predictable path for execution of commands. DMA enabled commands should be used during CQ operation, as there is no support to perform a direct mode read operation via the CQ.

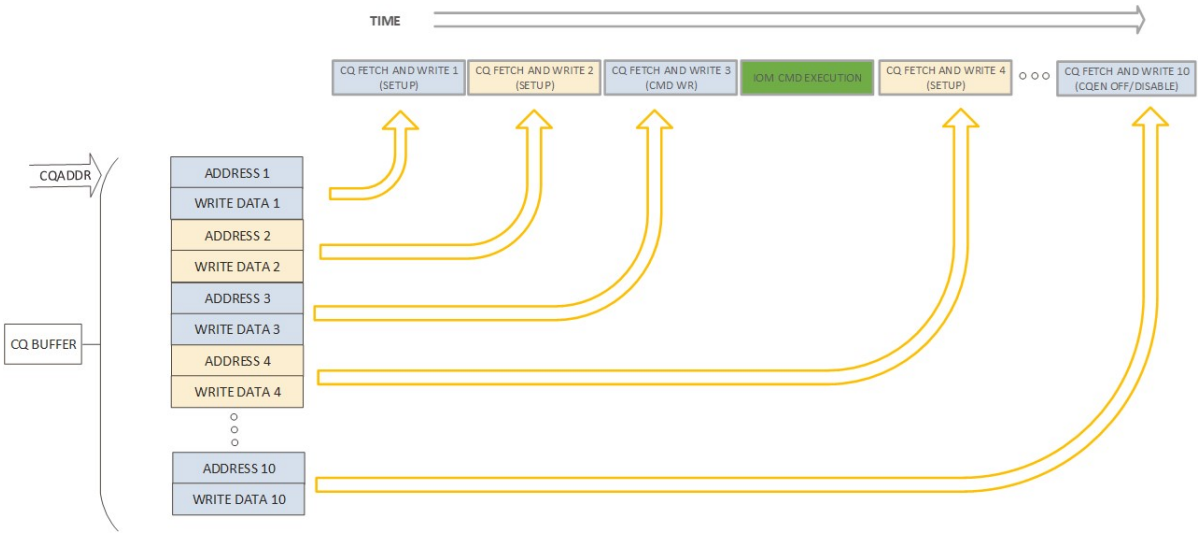

Figure 29. Register Write Data Fetches

The CQ starting fetch address is specified in the IOMn_CQADDR register. The CQ operation will start to fetch when the IOMn_CQCFG.CQEN field is set. This field should only be set when the IOM is idle and the FIFOs are empty. Once enabled, the CQ will continue to fetch sequentially until it encounters a pause event. A pause event can be caused by a CQ register write operation, or from external signals. This is shown in the sequence below.

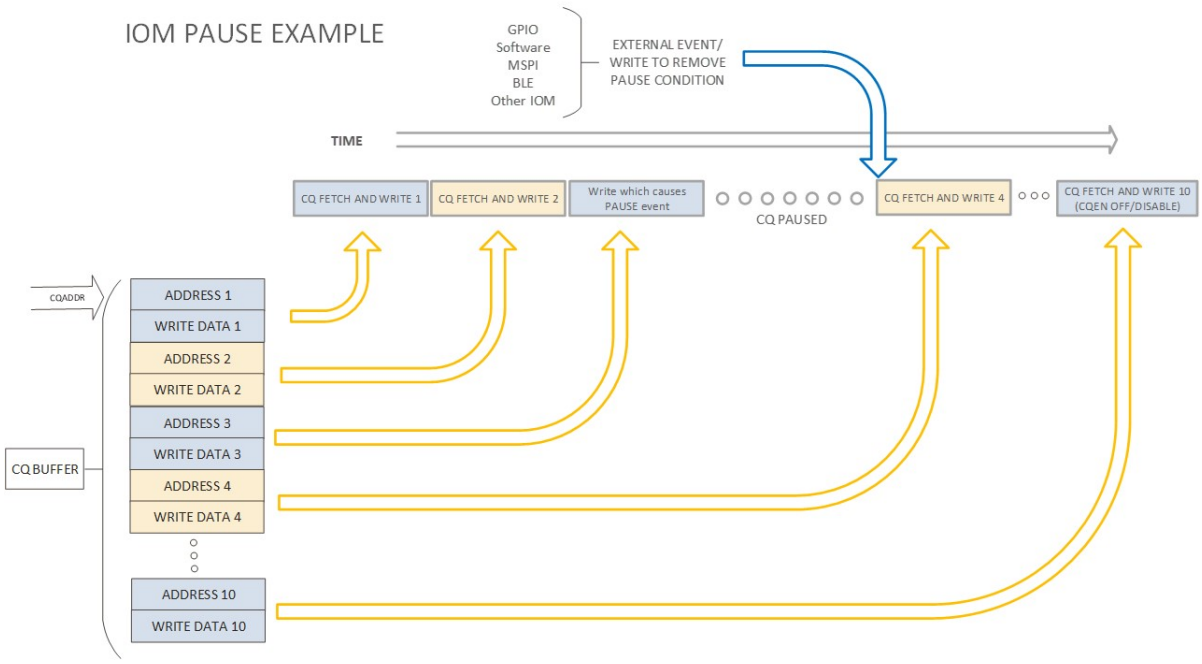

Figure 30. IOM Pause Example

Each pause source is independently enabled via the IOMn_PAUSEEN register. In addition to independent enable of the pause bits, there is also independent control of which pause event will signal a CQPAUSE interrupt. This is controlled through the IOMn_CQFLAGS.CQIRQMASK field.

There are 16 possible pause sources. When the value of the pause source is set, and the pause is enabled in the IOMn_PAUSEEN register, the CQ will stop fetching. The IOMn_CQADDR is updated after each fetch, and when paused, will point to the next doublet to be fetched when the pause condition is removed. The connection of the pause bits are shown below. The SW Flags are accessed via the IOMn_CQSETCLEAR register.

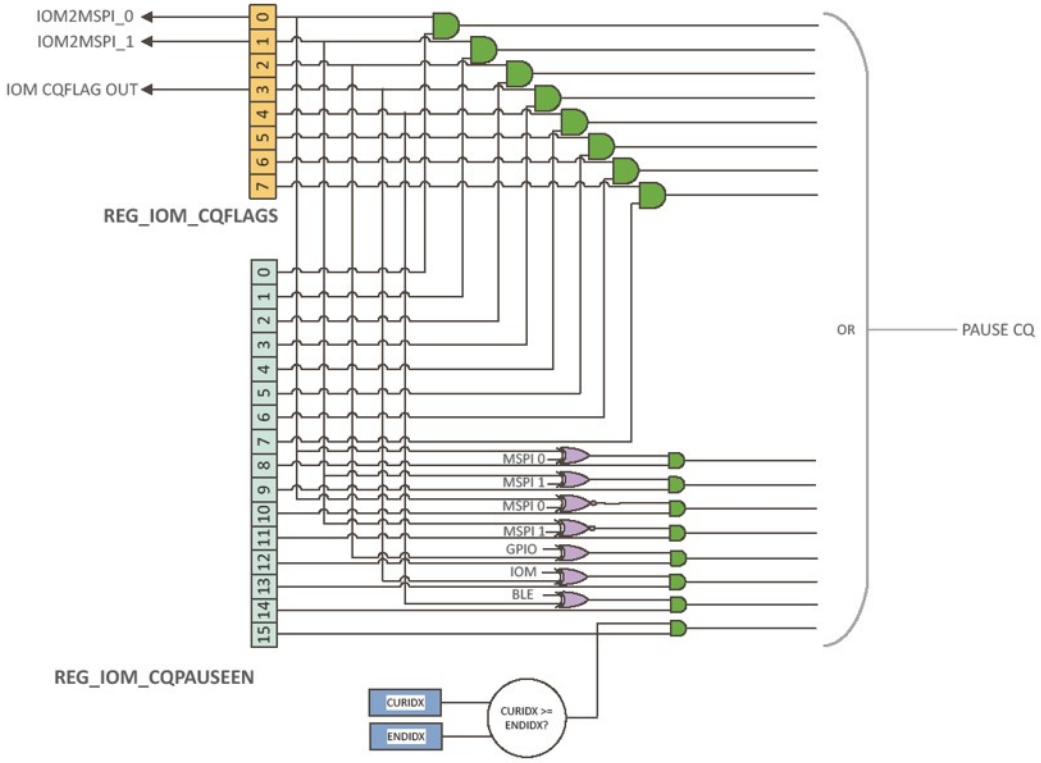

Figure 31. CQ Pause Bit Fetching

The first 8 pause sources (bits 7:0) are register bits which are directly writable via the MCU or through the CQ. These first 8 locations are called SW Flags. Because the CQ does not support a read-modify-write operation, special facilities are available to set, reset or toggle the SW Flags. This is accessed through the IOMn_CQSETCLEAR register. The 3 fields in this register allow a per bit set, reset or toggle of the SW Flag bits.

The next 7 pause sources (bits 14:8) use the SW Flags along with an external signal to set the pause event. The external signals are from the GPIO module, the MSPI module, or other IOM modules. On some cases, such as the MSPI interface, 4 of the SW Flags are used and combined with 2 similar signals from the MSPI module to facilitate a ping pong method of sharing 2 buffers and preventing overruns without MCU intervention.

The last pause source (bit 15) is used for index pausing. If this pause bit is enabled, the CQ will pause when the value of the IOMn_CURIDX matches the IOMn_ENDIDX. This is useful for software to be able to update the CQ buffer without causing a race condition between the CQ data buffer writes and the CQ fetches.

17.5.1 CQ Programming Notes

Following are some points to consider when programming command queue operation.

- Additional restrictions when using the CQ function is that the DMA must be disabled prior to writing the IOMn_CQADDR register, either from the MCU or from the CQ itself.
- For multiple commands using DMA, the DMAEN must be reset after the command is done and before the DMA registers are set for the next transaction.
- It is possible for the CQ to write the IOMn_CQADDR register during the CQ operation. The new address will take effect on the next fetch and allows the CQ to be relocated or looped.

- When starting the CQ operation, 1 doublet will be fetched regardless of the state of the pause status and bits. If any pause is active, it will take effect after the first fetch. For this reason, it is generally advisable to have a dummy register write as the first CQ doublet.

CQ write operations to SW flags used in combination with pause events 15:8 must first disable the pause enable, perform the SW flag write, then re-enable the pause enable register. SW flags 7:0 can be written without this restriction and will cause a pause immediately if activated.

17.6 Additional Information

Please refer to the IOM registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

18. Improved Inter-Integrated Circuit (I3C) Host

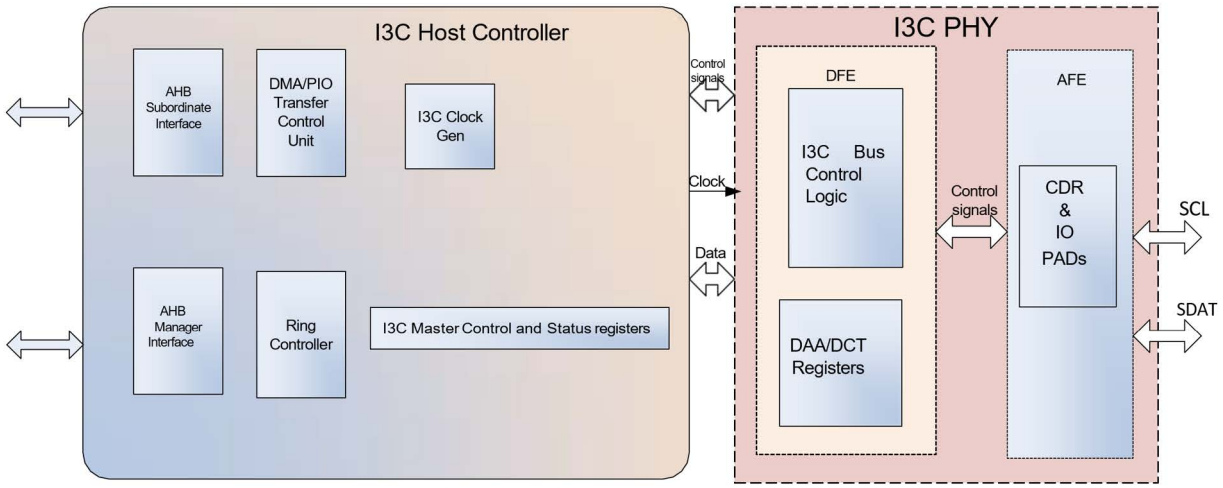

Figure 32. I3C Host Block Diagram

18.1 Features

The Improved Inter-Integrated Circuit (I3C) Host Controller supports features shown in Figure 32 and listed below.

- Compliant with MIPI I3C Specification (v1.1.1)
- Compliant with MIPI I3C HCI Specification (v1.1)
  - PIO and DMA mode
  - At least four rings support in DMA mode
- Supports up to 12.5 MHz operation using Push-Pull
- Open-Drain and Push-pull type transactions
- Supports legacy I^2C devices
- Dynamic Addressing while supporting Static Addressing for Legacy I^2C devices
  - At least three devices with dynamic addressing
- Legacy I^2C Messaging
- I^2C-like Single Data Rate Messaging (SDR)
- High Data Rate Messaging Modes (HDR-TSP and HDR-TSL)
- Reception of In-band Interrupt support from the I3C subordinate devices
- Reception of Hot-Join from newly added I3C subordinate devices
- Support for JESD403-1 Sideband Bus Interfaces

18.2 Functional Overview

The Apollo510 Lite SoC includes an I3C Host Controller that implements controller functionality as defined by the MIPI Alliance's I3C Specification. The I3C Host Controller implements support for:

- Legacy I^2C subordinate devices
- Clock frequency scaling
- Open drain and push-pull operation of the I3C Interface
- Dynamic addressing support

The I3C Host Controller supports the required SDR mode at clock frequencies up to 12.5 MHz, as well as HDR modes (HDR-TSP and HDR-TSL) as defined by the I3C Specification.

Figure 32 shows the architectural block diagram of the I3C Host controller core, where the manager interface is used for DMA mode transfers. The sub-modules in the diagram function as described below.

I3C Control and Status Registers

Implements the Configuration, Control, and Status Registers and Data FIFO Interface Registers which are accessible through the AHB Target Interface.

This module implements the Interrupt Generation logic to the AHB Interface based on the enabled interrupts (FIFO Status, or Transaction Complete). It also provided an access to the Data FIFO using the Data Port Registers.

I3C Clock Gen

Generates the I3C Clock (SCL) from the I3C Reference Clock. The ratio of the SCL is auto-chosen based on the mode of operation required. Also the I3C manager state machine will use this module to scale the SCL during certain transactions.

DMA/PIO Controller

Implements the functions required to interact between the Host and manager control state machine. For PIO mode this includes the register array for the data transactions, IBI request/status.

Ring Controller

Interacts with the register control and AHB manager interface to read/write the data from/to the system memory. This module includes an arbiter to switch the command processing across different enabled ring.

AHB Subordinate Interface

Used by an external application to configure and control the I3C Controller and can be used to transfer data to/from the FIFOs. This interface supports only a single transaction (non-burst).

AHB Manager Interface

Used to transfer data using the DMA engine.

I3C PHY - Transmitter and Receiver

The I3C driver operates in two modes: Push-Pull Mode and Open Drain Mode. In Push-Pull Mode, the SDA pin drives at higher speeds with a totem-pole driver.

See I3C DC I/O stage specifications in the Electrical Specifications - “Improved Inter-Integrated Circuit (I3C) Host” on page 241.

18.3 Additional Information

Please refer to the I3C registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

19. Full Duplex SPI Subordinate (IOSFD)

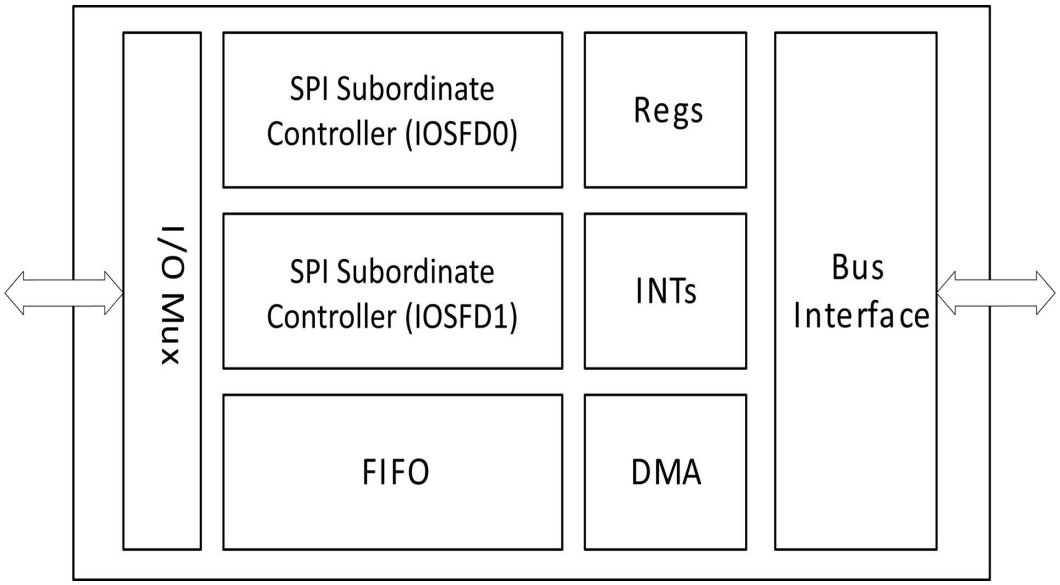

Figure 33. Full Duplex IOS SPI Subordinate Controller Pair (IOSFD0 / IOSFD1)

19.1 Features

The Apollo510 Lite SoC includes two instances of the Full Duplex SPI Subordinate and both instances are designed to work in tandem to enable full duplex (FD) operation. Features of the controller pair are shown in Figure 33 and listed below.

- Functions as a synchronous communications subordinate in a SPI configuration
- Supports DMA mode
  - DMA total transfer count support for 64 kB data
  - Supports DMA complete and DMA error interrupts
- Supports full duplex operation when both instances are used in combination (only IOSFD0 is pinned out)
- IOSFD0 instance can work independently to provide half duplex operation
- May be placed in a sleep mode and still operate over the I/O interface
- Each controller contains 64 bytes of Local RAM (LRAM) maintained in deep sleep mode for data/parameter storage, which can be configured flexibly as three operational blocks
- Extensive set of interrupts to control data flow and command processing, and provide alerts for writes to various locations

NOTE

Restrictions on IOSFD operation:

1. Simultaneous DMA read and write operations are not supported for IOSFD configured for half duplex. The DMA transfer direction should be configured properly.
2. Command Queue is not supported for IOSFD.
3. DMA mode is supported only for IOSFD FIFO mode (Host read/write to IO address 0x7F).

19.2 Functional Overview

The Apollo510 Lite SoC includes two instances of the Full Duplex SPI Subordinate module, IOSFD0 and IOSFD1, which in combination support full duplex operation. Only SPI mode is supported in the IOSFD module, and it supports all polarity/phase combinations and interface frequencies as specified in the Serial Peripheral Interface (SPI) Subordinate Interface sub-section of the Electricals. The IOSFD0 module can function as a half duplex SPI interface. The device may be placed in a sleep mode and still receive operations over the I/O interface. The subordinate may be configured to generate an interrupt on specific references.

Each IOSFD instance contains 64 bytes of LRAM which is only accessible when the module is enabled. This RAM may be flexibly configured into three spaces:

- A block directly accessible via the I/O interface.
- A block which functions as a FIFO for read operations on the interface. This area is required because DMA transfers must utilize the FIFO.
- A block of generally accessible RAM used to store parameters during deep sleep mode. Although this can be configured for use in IOSFD, it is not recommended.

19.3 Full Duplex DMA Features

The IOSFD interface connection options are configured on the following pads with the functions selected with the Function Select (FNCSEL) values as shown:

- GPIO0 (FNCSEL = 1) & GPIO102 (FNCSEL = 0) - SLFDSCK - the input SPI clock which is connected to both IOSFD0 and IOSFD1
- GPIO1 (FNCSEL = 1) & GPIO103 (FNCSEL = 0) - SLFDMOSI - the input SPI data which is connected to both IOSFD0 and IOSFD1
- GPIO1 (FNCSEL = 10) & GPIO103 (FNCSEL = 1) - SLFDSDAWIR3 - the bidirectional SPI data in/out which is connected to IOSFD0
- GPIO2 (FNCSEL = 1) & GPIO104 (FNCSEL = 0) - SLFDMISO - the output SPI data which is connected to IOSFD0
- GPIO3 (FNCSEL = 1) & GPIO105 (FNCSEL = 0) - SLFDnCE - the input nCE which is connected to both IOSFD0 and IOSFD1
- GPIO4 (FNCSEL = 1) & GPIO106 (FNCSEL = 0) - SLFDINT - the interrupt out which is connected to IOSFD0

In normal operation, GPIO2 is connected to IOSFD0 and IOSFD0 is configured to execute a DMA write transaction (DMACFGn_DMADIR = 0). IOSFD1 is configured to execute a DMA read transaction (DMACFGn_DMADIR = 1). Separate memory addresses (in DMATARGADDR_TARGADDR) must be configured in the two IOSFD modules, but the transfer length DMATOTCOUNT_TOTCOUNT may or may not be the same in both modules. Once the modules are enabled, they both respond independently to a full duplex transfer on the interface, with the read and write DMA operations proceeding in parallel. DMA completion and error interrupts will typically occur in both modules simultaneously.

Configuring a full duplex DMA environment involves several steps:

1. Configure the pinmux to connect the four IOSFD pads to both IOSFD0 and IOSFD1, with IOSFD0 supplying the MISO signal and executing the DMA write and IOSFD1 executing the DMA read.

   [Note that the DMA direction is the opposite of the interface direction, which may be confusing. On a DMA write, data is read over the interface (using MISO) and written to memory. On a DMA read, data is read from memory and written over the interface (using MOSI).]

2. Set DMADIR to 0 in IOSFD0 and to 1 in IOSFD1.
3. Set the DMACFG_FRCDMA bit to 1 in both modules. Set the DMACFG_FRCRDWRT bit to 1 in IOSFD0 and to 0 in IOSFD1.

4. Set the DMACFG_PADBYTEEN bit to 1 in IOSFD0 and configure the desired DMACFG_PADBYTE value. These fields can also be set in IOSFD1 but have no effect on DMA reads.

The Host must send an address byte at the beginning of the transfer, but the R/W bit is ignored and each IOSFD module executes the desired transfer.

Figure 34 shows the basic environment and test structures. A full duplex configuration is shown.

19.4 Full Duplex DMA Transfers in SPI Mode

Full duplex transfers are implemented by configuring a DMA read in one IOSFD (IOSFD1 in Figure 34) and a DMA write in the other IOSFD module (IOSFD0 in Figure 34). The configurations force IOSFD1 to treat the transfer as a read and IOSFD0 to treat the transfer as a write, independent of the R/W bit. Both modules are connected to SCK and nCE so they execute a synchronized transfer. The Host sends the DMA read data on MOSI (to IOSFD1) and receives the DMA write data on MISO (from IOSFD0).

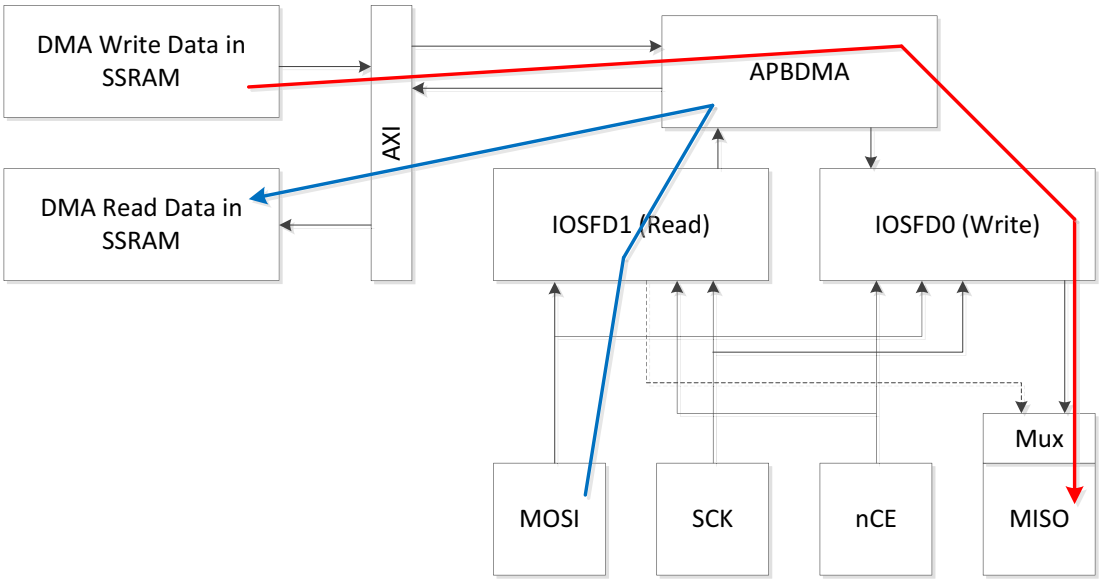

Figure 34. Full Duplex IOS DMA Transfers in SPI Mode

19.5 Half Duplex DMA Reads in SPI Mode

Half duplex DMA reads use the data flow path shown by the blue arrow in Figure 35.

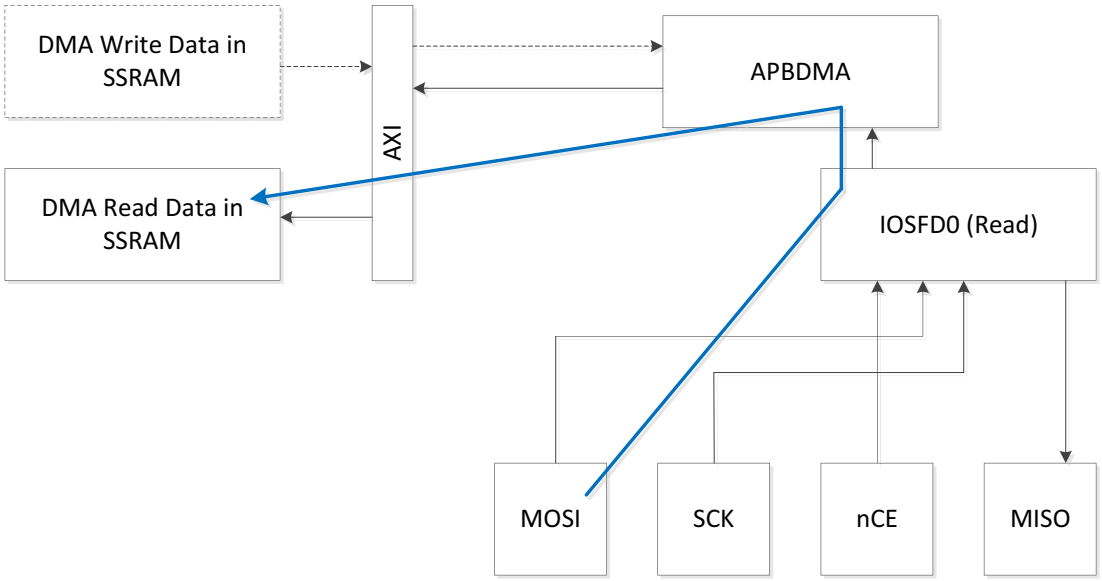

Figure 35. Half Duplex IOS DMA Reads in SPI Mode

Once the DMA transfer is configured in the IOSFD0 module, the Host initiates a write transfer, generating the clock SCK and the chip enable nCE with data coming in on the MOSI pad. The transfer address must be the FIFO address 0x7F. The data flows through the IOSFD FIFO in the LRAM, and the APBDMA Controller reads that data over the APB and writes it into the target memory (such as SSRAM0) via the AXI bus.

19.6 Half Duplex DMA Writes in SPI Mode

Half duplex DMA writes by the IOSFD0 module use the data path shown by the red arrow in Figure 36.

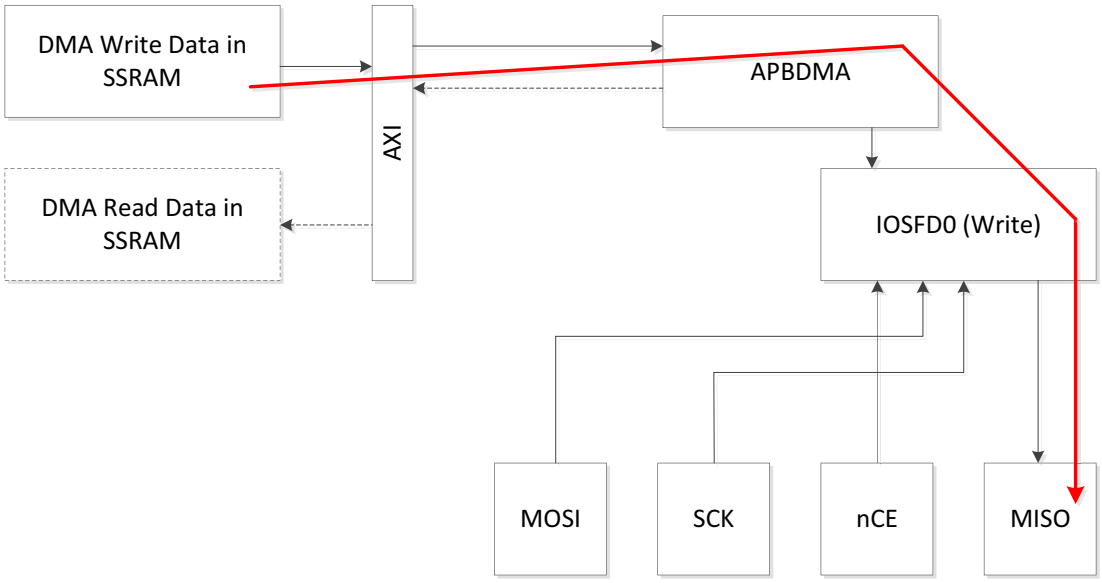

Figure 36. Half Duplex IOS DMA Writes in SPI Mode

IOSFD0 makes DMA requests and the APBDMA controller transfers data from the source memory (such as SSRAM1) via the AXI bus to the IOSFD0 FIFO in the LRAM. The Host initiates a read transfer, generating the clock SCK and the chip enable nCE with data flowing out of IOSFD0 on the MISO pad. The transfer address must be the FIFO address 0x7F.

19.7 IOSFD DMA Registers

Several registers are included in the IOSFDn register set to support DMA operations. Please refer to the IOSFD registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

19.8 IOSFD LRAM Configuration for DMA

The first step in configuring the IOSFD is to allocate the LRAM memory regions. Since we often want the Host to be able to transfer commands into the IOSFD, we typically assign a small part of memory, i.e., 8 or 16 bytes, as the Direct region by setting FIFOBASE to 1 or 2. We can then use the REGACC interrupts to signal the CPU that there is a command available. If we don't need any LRAM area, which is by far the most common case, the remaining LRAM is typically assigned to the FIFO area by setting FIFOMAX to 32. All DMA transfers will go through the FIFO area. If the Direct Area of memory is not used, FIFOBASE can be set to 0 to maximize the size of the FIFO.

The IOSFD modules, IOSFD0 and IOSFD1, contain 64 bytes of LRAM each. FIFOMAX must be 8 or less, and FIFOBASE must be small enough to configure at least 48 bytes of FIFO space.

19.9 Executing a DMA Operation

An operation is initiated by the Host signaling to the MCU that a transfer will be executed, i.e., sending a command. This requires an interrupt to be generated to the CPU, waking it up if necessary, which can be done in several ways:

- Generating a hardware interrupt to the SLINT input pad from a Host pin.
- Generating a hardware interrupt to a GPIO input pad from a Host pin.
- Generating a software interrupt by writing to the HOST_WCS register in the IOSFD at address offset 0x7B.
- Generating a software interrupt by writing to the Direct memory area with the appropriate REGACC interrupt(s) configured. This is the recommended method.

Once the command has been detected, software on the CPU determines what the desired DMA parameters are - transfer direction, length and target address. Software then configures the DMA transfer in APB_DMA and IOSFD and starts the DMA operation. At this point the CPU must send a handshake signal to the Host indicating that the IOSFD is ready for the transfer. This handshake can be through a GPIO output pad to a Host pin.

When the Host detects that the IOSFD is ready for a transfer, it initiates a burst transfer (read or write) to the first address in the FIFO area, which is typically address offset 8 or 16. The Host then streams as much data as specified. The IOSFD transfers this data to or from the Host, and initiates DMA transfers as necessary to empty/refill the FIFO in the LRAM. The addresses in the LRAM rolls over from FIFOMAX-9 to FIFOBASE. When the DMATOTCOUNT_TOTCOUNT reaches 0, the operation terminates and a DMASTAT_DMACPL interrupt is generated.

After the operation is complete, the system waits for the receipt of another command from the Host, and the process continues.

19.10 Interrupt Processing

Two new interrupts, DCMP and DERR, are included in the IOSLAVEINT interrupt register. DCMP indicates the end of a DMA transfer, and the XCMPRR/XCMPRF and XCMPWR/XCMPWF interrupts are used as the Transfer Complete interrupts for read and write bursts respectively.

The DCMP interrupt (and the DMACPL status bit) is set when the DMA transfer completes, and the XCMPRF/XCMPWF interrupts (and the DMASTAT_XFRCMP status bit) is set when the IO transfer completes on the interface. In general software should enable the DCMP interrupt on P2M transfers (Peripheral-to-Manager, or DMA reads), and should enable the XCMPRF interrupt on M2P transfers (Manager-to-Peripheral, or DMA writes). The expected behavior is described in Table 23:

Table 23: DMA Interrupt Processing

DMADIR	Host-TOT	Interrupt	DMACPL	UNDFL	TOTCOUNT	DMAFSIZE	XCMPWF
0:P2M	==	DCMP	1	0	0	0	1
0:P2M	<	DCMP	1	0	Note 1	0	1
0:P2M	>	DCMP	1	0	0	Note 2	Note 2
1:M2P	==	XCMPRF	1	0	0	0	0
1:M2P	<	XCMPRF	Note 3	0	Note 4	Note 5	0
1:M2P	>	XCMPRF	1	1	0	Note 5	0

Table Notes:

Note 1: (Initial TOTCOUNT - Final TOTCOUNT) = number of bytes written to memory.

Note 2: If XCMPRF = 1, if DMAFOVF = 0, DMAFSIZE contains the number of valid bytes in the FIFO which were received from the Host but not written to memory. If DMAFOVF = 1, the number of valid bytes in the FIFO is unknown because the FIFO has been overwritten. It is possible that for a very slow interface executing a very long transfer, XCMPF will still be 0 when the DCMP interrupt is serviced. If software needs the remaining FIFO information it must wait until XCMPRF becomes 1 to read DMAFSIZE and DMAFOVF.

Note 3: If the Host interface is very fast, the internal buses are heavily utilized and the CPU responds very quickly to interrupts. There is a very small probability that DMACPL is not asserted when the XCMPRF interrupt is received. But in any case, it will be set soon after that.

Note 4: (Initial TOTCOUNT - Final TOTCOUNT) = number of bytes read from memory. This will be more data than was actually transferred on the Host interface and is not a useful value.

Note 5: DMAFSIZE is not valid.

The XFRCOUNT register field contains the number of bytes actually transferred on the interface on a DMA read, and the number of bytes actually transferred + 1 on the interface on a DMA write or in the write IOSFD in a full duplex transfer. This is very useful in determining any “extra” data in the FIFO at the completion of an operation.

For a full duplex transfer, the terminating interrupt should be DCMP on the IOSFD that is implementing the DMA read, which is typically iOSFD1. The status values in each IOSFD is a function of the configured DMA length, which may be different in each IOSFD, and the Host transfer length, which is the same in both IOSFDs.

19.11 Full Duplex DMA Processing

At the completion of each DMA operation, after reading all relevant status information, DMAEN should be set low. This will reset many of the status register bits and prepare the module for the next operation. All configuration fields should be written and all status and interrupt bits cleared *before* DMAEN is set to 1.

For full duplex transfers, the following sequence should be used. This assumes IOSFD0 is implementing the DMA write and IOSFD1 is implementing the DMA read.

1. Make sure DMAEN is clear in IOSFD0 and IOSFD1.
2. Configure each IOSFD instances for its respective transfer. Clear any writable status bits like DMAUNDFL and DMAERR.
3. Enable the DCMP interrupt on IOSFD1. This will be the last interrupt status set on a correct transfer.
4. Set DMAEN for both IOSFD instances.
5. Wait for the DCMP interrupt from IOSFD1 (not from IOSFD0). At this point the Host should have read the correct data (not all PADBYTES).
6. The XCMPRF and DCMP interrupts should be set for IOSFD0, and the XCMPWF interrupt should be set for IOSFD1. These should be checked.
7. Read any status (TOTCOUNT, XFRCOUNT, etc.) to determine the transfer result.
8. Clear DMAEN for both IOSFD instances.

After DMAEN is set on the DMA read side (IOSFD1 in the typical case), the first transfer executed by the Host MUST be the actual full duplex transfer. The Host must not attempt to access any other interface address, such as the Direct Address space or the IOINT module.

Once the interface transfer is complete, the Host may then access other offsets within the IOSFD. These accesses (reads and writes) will all go to the IOSFD configured for the DMA write transfer (IOSFD0 in the typical case). No interface accesses will occur to the other IOSFD module.

19.12 Additional Information

Please refer to the IOSFD registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

20. Universal Asynchronous Receiver/Transmitter (UART)

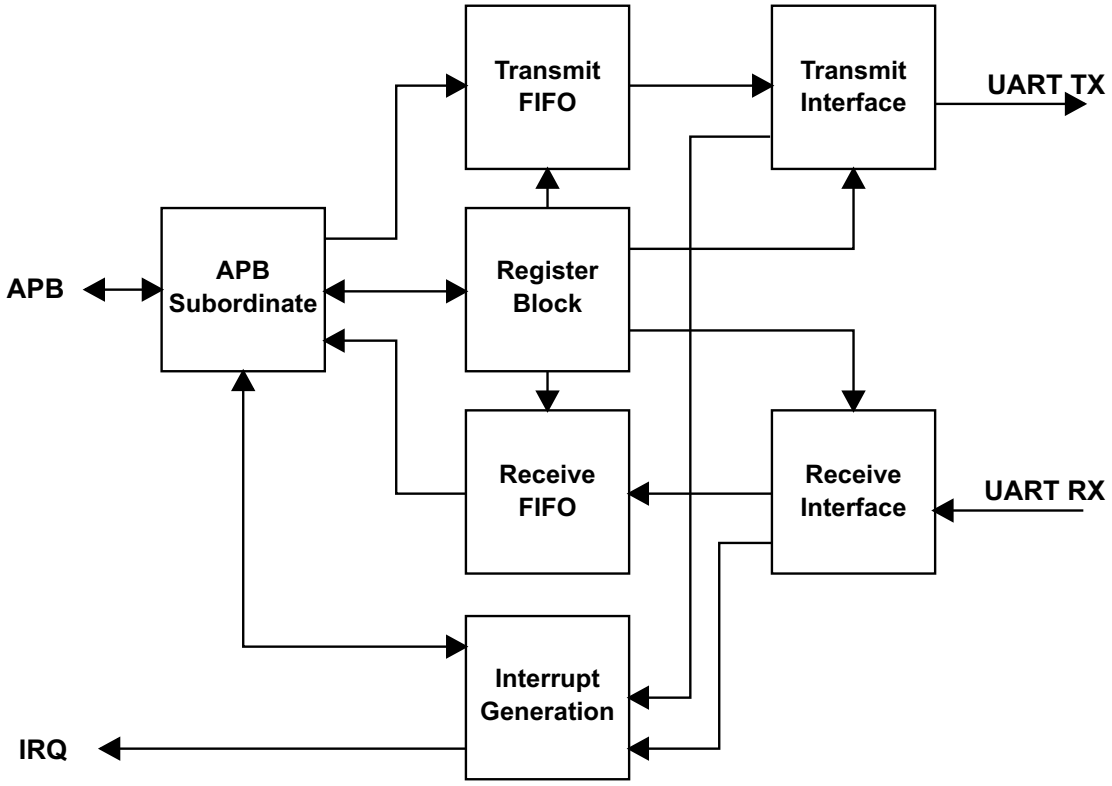

Figure 37. UART Block Diagram

20.1 Features

The Universal Asynchronous Receiver/Transmitter (UART) includes features shown in Figure 37 and listed below.

There are two (2) Universal Asynchronous Receiver/Transmitter (UART) instances on the Apollo510 Lite SoC. The UART Module includes the following key features:

- Operates independently, allowing the MCU to enter a low power sleep mode during communication
- 32 x 8 transmit FIFO and 32 x 12 receive FIFO to reduce MCU computational load
- Programmable baud rate generator
- Fully programmable data size, parity, and stop bit length
- Programmable hardware flow control
- Support for full-duplex and half-duplex communication
- Supports DMA (half-duplex mode only)
- Loop-back functionality for diagnostics and testing

NOTE

Since UART DMA is only supported in half-duplex mode, two UART instances are required (one for TX and one for RX) to support full-duplex DMA. In this full-duplex mode, the TX instance should be configured to use 2 stop bits and the one for RX should use 1 stop bit setting. The external UART TX needs to use 2 stop bits setting.

20.2 Functional Overview

Each UART converts parallel data written through the APB Subordinate port into serial data which is transmitted to an external device. It also receives serial data from an external device and converts it to parallel data, which is then stored in a buffer until the CPU reads the data.

The UART module includes a programmable baud rate generator which is capable of operating at high baud rates. An interrupt generator optionally sends interrupts to the CPU core for transmit, receive and error events.

Internally, the UART module maintains two FIFOs. The transmit FIFO is 1-byte wide with 32 locations. The receive FIFO is 12-bits wide with 32 locations. The extra four bits in the receive FIFO are used to capture any error status information that the Apollo510 Lite SoC needs to analyze.

NOTE

In accordance with the PC16550 UART specifications, the CTS interrupt triggers (when enabled) if the state of the CTS input changes from low to high or from high to low. Additionally, if the CTS input is high during the initialization and enabling of the UART, the CTS interrupt will be triggered. Software should handle such interrupt events appropriately.

20.3 Additional Information

Please refer to the UART registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

21. Universal Serial Bus (USB)

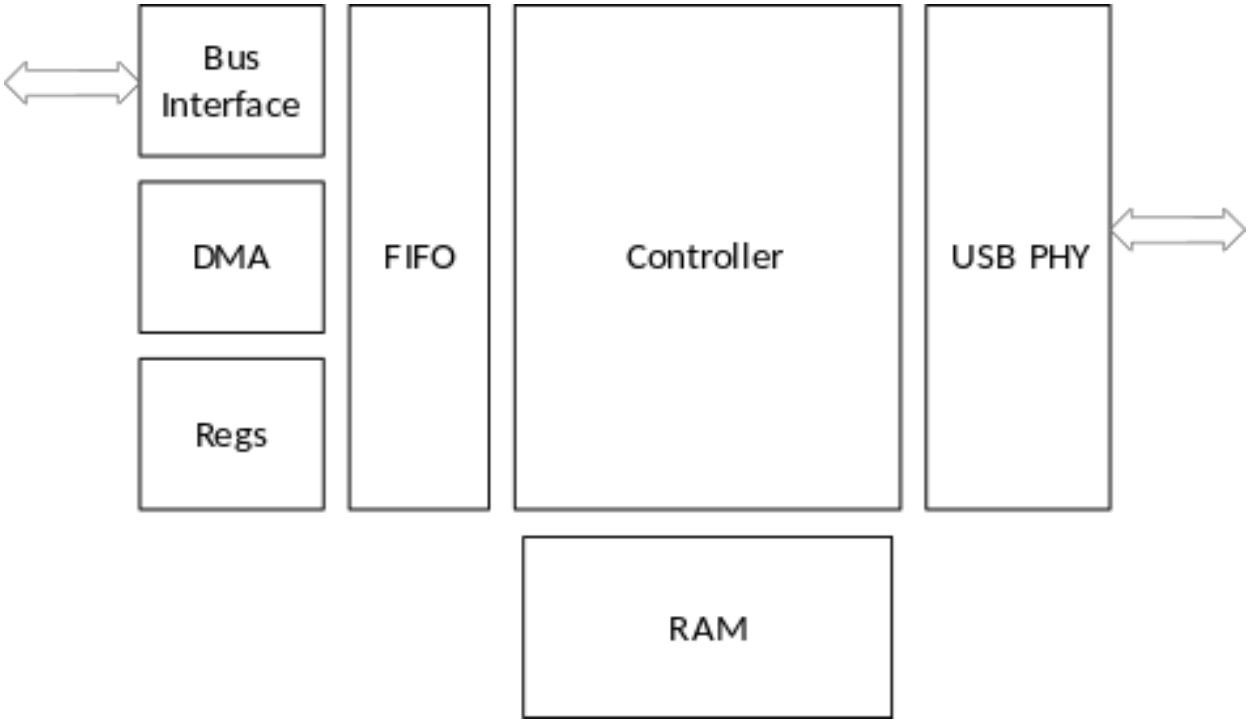

Figure 38. USB Block Diagram

21.1 Features

The Universal Serial Bus (USB) Subsystem includes features shown in Figure 38 and listed below.

- USB 2.0 FS/HS Device Mode
- Dynamic FIFO sizing: 4 kB total FIFO
- IN endpoints: 5
- OUT endpoints: 5
- IN bulk packet splitting supported
- OUT bulk packet combining supported
- Concurrent DMA supported for all IN/OUT BULK endpoints
- Soft connect/disconnect supported
- Suspend mode
- Supported classes
  - Communication Device Class (CDC)
  - Mass Storage Class (MSC)
  - Device Firmware Upgrade (DFU) Class
  - Human Interface Device (HID) Class
- Charging Support
  - Battery Charging 1.2 (BC1.2) supported for battery charger detection
  - Selected 3rd-party proprietary charger detection supported

21.2 Functional Overview

The USB subsystem provides support for USB 2.0 Full Speed (12 Mbps) and High Speed (480 Mbps) interface. This interface is primarily used for bulk data transfer, firmware updates and charging detect.

The USB controller supports up to 5 IN / 5 OUT endpoints plus 1 control. The FIFO sizing for each endpoint is dynamically configurable up to 4 kB, with the restriction that IN and OUT port sizing must be up to half the total FIFO size. The controller also supports DMA transfers to/from system memory.

The Apollo510 Lite SoC has an integrated USB 2.0 PHY with support for Suspend Mode operation. Battery charger detection is supported within the PHY to enable battery charge algorithm execution and control of the external battery charge / power management IC. The charger detection supports Battery Charging Specification 1.2 (BC1.2) as well as the majority of proprietary (non-BC1.2 standard) chargers.

21.3 Power States

The USB subsystem supports power states as shown in Figure 39 and described below.

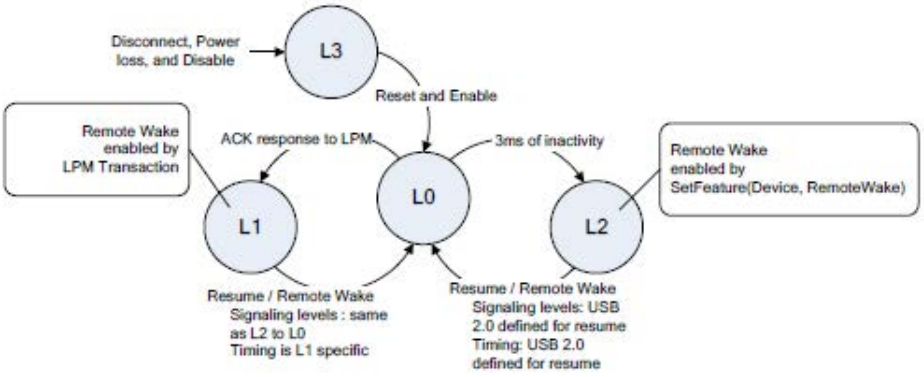

Figure 39. USB Power States Transitioning Diagram

L0 (On)

In this state, the port is enabled for propagation of transaction signaling traffic. A port in L0 is either actively transmitting or receiving data (L0-Active) or able to do so but not currently transmitting or receiving information (L0-Idle). While in this state Start-of-Frame (SOF) packets are issued by the host at a rate corresponding to the speed of the client device (1 ms for full-speed, 125 µs for high-speed). Note, the host transmits keep-alives or the USB 2.0 hub translates some SOFs into keep alives if the device connected on the downstream port is a Low-speed device. The line state during L0-Active and L0-Idle vary according link speed as does the mechanism by which the host detects device hot-removal (e.g. during SOF phase for high-speed devices). Entry to L0 is via reset or resume signaling (either from L1 or L2).

L1 (Sleep)

The L1 (Sleep) state is not supported on the Apollo510 Lite SoC.

L2 (Suspend)

This is the formalized name for USB 2.0 Suspend, see Section 7.1.7.6 in the USB 2.0 specification. Entry to L2 is nominally triggered by a command to a hub or host port to transition to suspend, at which point the port ceases repeating signaling down the port (and may transition the port out of high-speed mode). The device discovers the suspend condition via observing 3ms of inactivity. The resultant line state is either Low or Full-speed idle. L2 also imposes power draw requirements (from VBUS) on the attached device. Exit from this state is via remote wake, resume signaling, reset signaling or disconnect.

L3 (Off)

In this state, the port is not capable of performing any data signaling. It corresponds to the powered-off, disconnected, and disabled states. The L3 state is transitioned to when the Apollo510 Lite SoC receives an assertion or deassertion of the “PowerOK” signal from the Power Management / Charger IC.

21.4 Hardware Design Guidelines

The following sub-sections provide design guidelines for the use of the USB Controller and PHY. Please consult the USB section of the Electricals for voltage, power and timing requirements of the PHY.

21.4.1 Battery Charger Detection

Charger detection capabilities are as follows:

- Dedicated Charging Port (DCP) as per Battery Charging Specification Version 1.2 (BC1.2)
- Charging Downstream Port (CDP) as per BC1.2
- Standard Downstream Port (SDP) as per BC1.2
- Custom Charger

Not supported and/or non-applicable BC 1.2 features are listed below.

- OTG device
- Accessory Charger Adapter (ACA)
- ACA-Dock
- SuperSpeed Consideration
- Personal System 2 (PS2) - PHY DP/DM pads do not tolerate 5V

21.4.1.1 Battery Charger Detection during USB Connection

Charger detection during USB connection follows the flow shown in Figure 40.

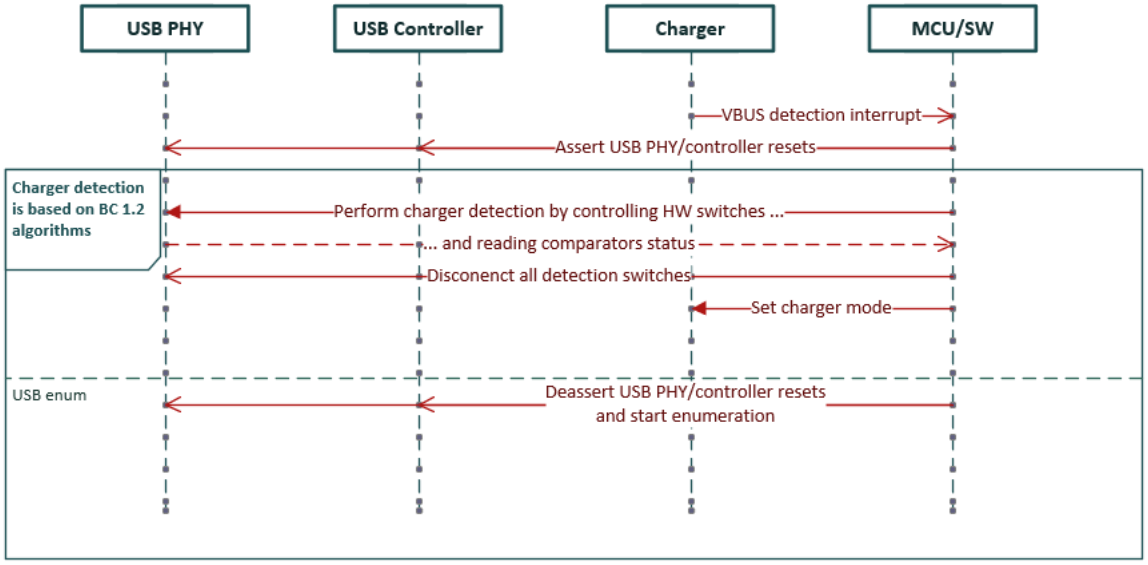

Figure 40. Charger Detection in USB Connection Flow

The charging detection algorithm in Figure 41 is based on the BC 1.2 specification. Weak Battery Algorithm (Figure 42) and Good Battery Algorithm (Figure 43) should be implemented in an interrupt-driven manner to take full advantage of the device's power saving features. Note that debouncing software timers and their interrupts are not shown in the diagram for clarity, but must be implemented according to BC 1.2 specification.

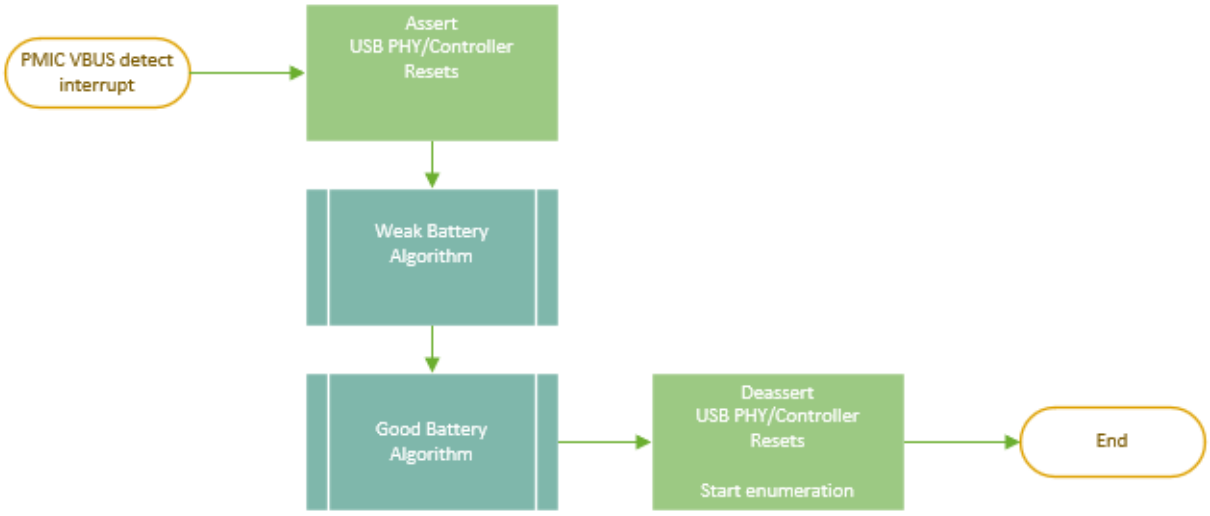

Figure 41. Charging Detection Algorithm

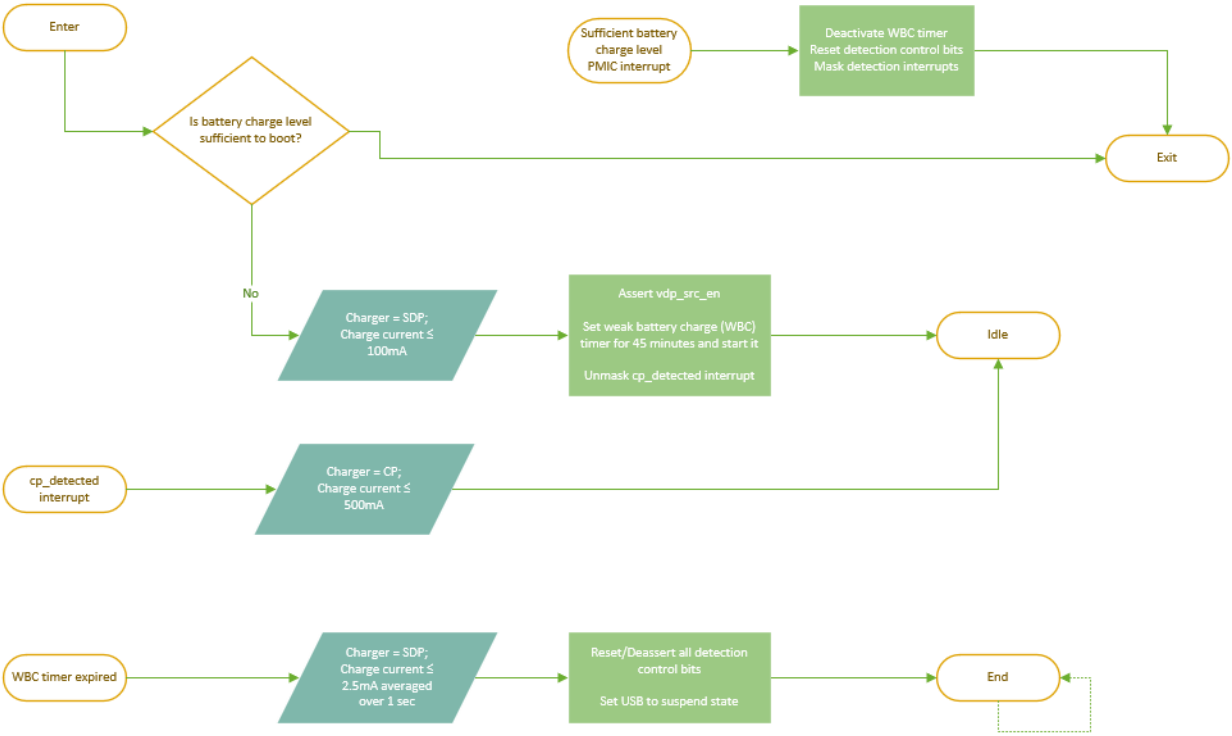

Figure 42. Interrupt-driven Weak Battery Algorithm

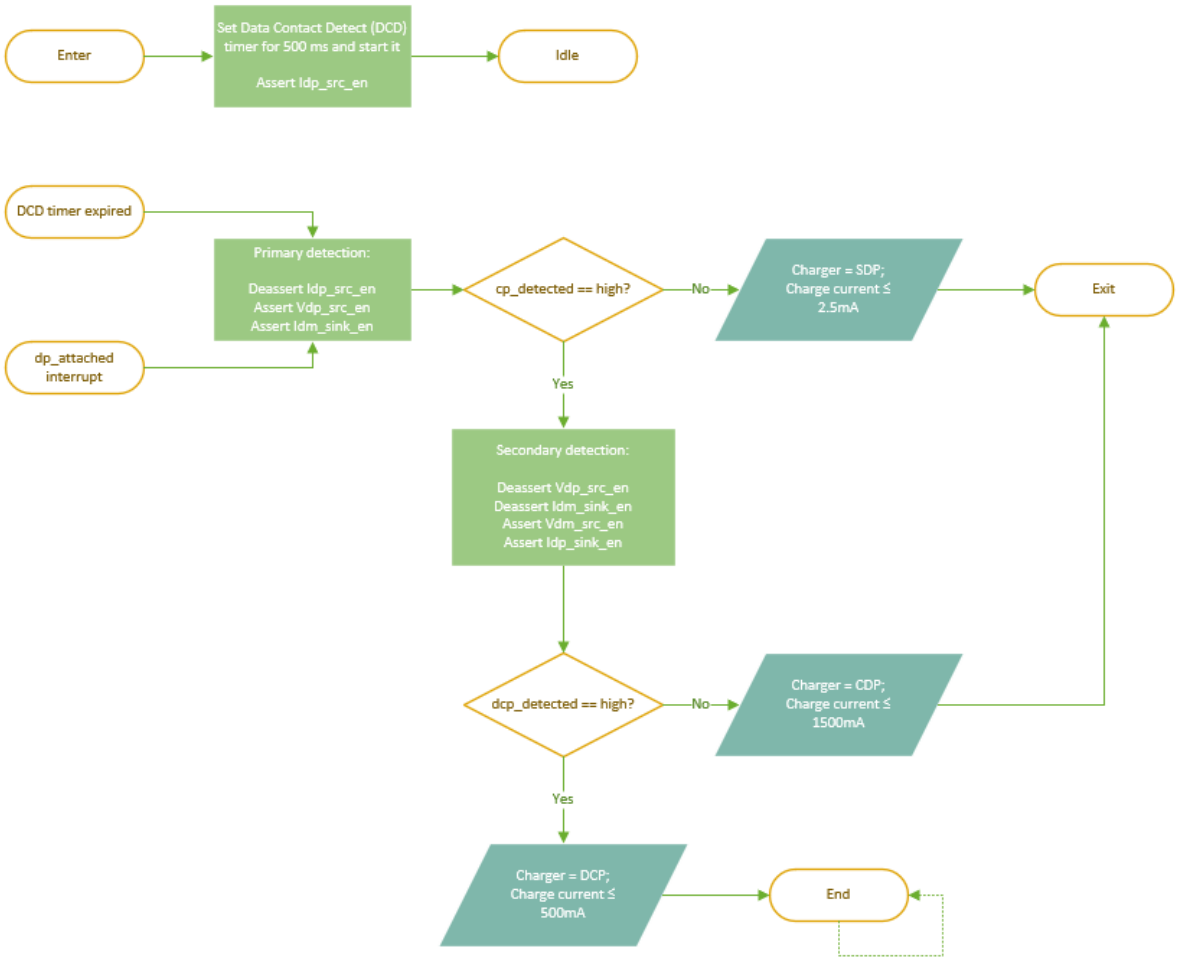

Figure 43. Interrupt-driven Good Battery Algorithm

Charger detection algorithms should take into account timings between assertion/deassertion control signal and status signal change as shown in Figure 44.

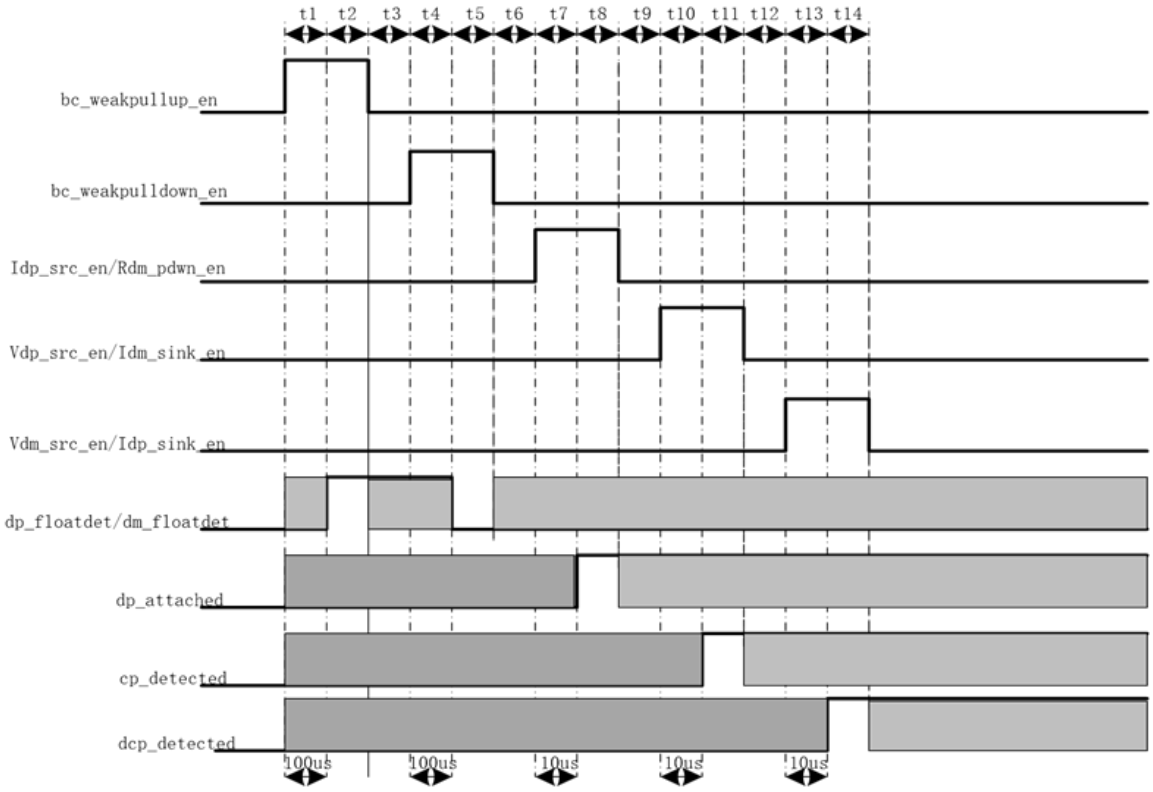

Figure 44. Battery Charging Sequence

21.4.2 System Power Sequencing for USB

The power sequence for the relevant power supplies is contingent on the PHY(s) used in the system. The sections below cover the case for the USB PHY and addresses the proper sequence which includes powering the VDDUSB33 (3.3 V) and VDDUSB0P9 (0.9 V) supplies.

Apollo510 Lite SoC's USB in the user system requires the following:

1. Allocation of the wake-up capable GPIO for VBUS detect
2. Powering USB PHY 3.3V rail from the VBUS-sourced DC/DC to prevent power losses when USB is not in use

USB power-on sequence:

1. VBUS detect GPIO assertion (concurrent with 3.3v ramp) results in CPU wakeup
2. USB software driver/stack initializes USB with the following sequence
   A. Disable USB LDO active discharge
   B. Enable USB LDO
   C. Sleep for the max USB LDO start-up time
   D. Enable PD_USB and PD_USBPHY
   E. Perform USB configuration/enumeration

USB power-off sequence:

1. USB software driver/stack power off USB with the following sequence
   A. Disable PD_USB and PD_USBPHY
   B. Disable USB LDO

C. Enable USB LDO active discharge

Refer to the USB PHY section in the Electricals for supply voltage specifications.

21.5 Additional Information

Please refer to the USB and USBPHY registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

22. Secure Digital Input Output (SDIO)

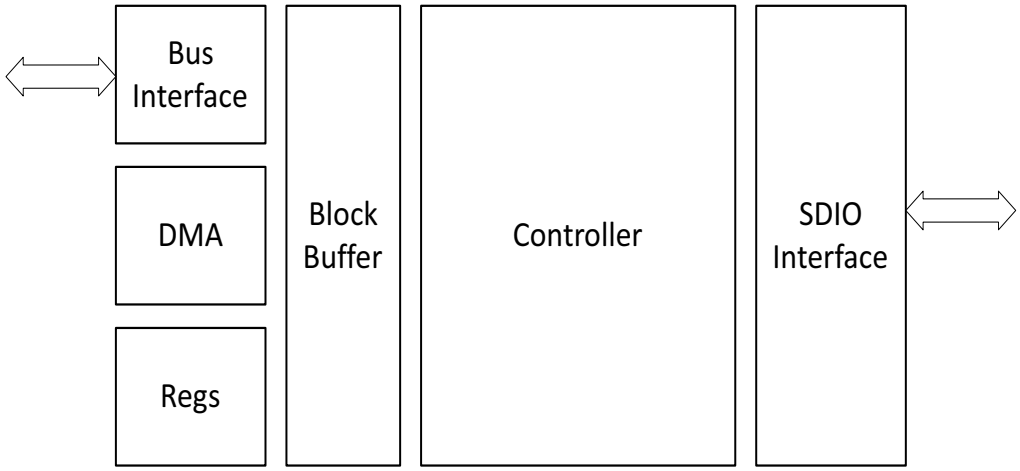

Figure 45. SDIO Block Diagram

22.1 Features

The Secure Digital Input Output (SDIO) Module includes features shown in Figure 45 and listed below.

- 2x SDIO Controller instances allowing for concurrent eMMC and SDIO interface support
- SDIO card specification Version 3.0
- Host clock rate variable between 0 and 96 MHz
- Up to 48 MB/s data rate using 4 parallel data lines (SDR50/DDR50 mode)
- Transfers data in 1-bit and 4-bit SD modes
- Transfers data in SDR50 or DDR50 modes
- SDIO0 and SDIO1 transfer data in 8-bit eMMC mode for 96 MB/s maximum transfer rate
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
- Variable-length data transfers
- Performs Read Wait Control, Suspend/Resume operation

22.2 Functional Overview

The SDIO host controller provides support for higher bandwidth device transfer. A typical application is for Wi-Fi IC connectivity. The SDIO controller supports up to 2 kB block buffering as well as dedicated DMA controller support to provide maximum host offload. The DMA algorithm supported is the Advanced DMA version 2 (ADMA2) which allows for flexibility in memory allocation. The controller interface supports a programmable DLL to allow for timing tuning for optimal windowing.

22.3 Additional Information

Please refer to the SDIO registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

23. Display Subsystem

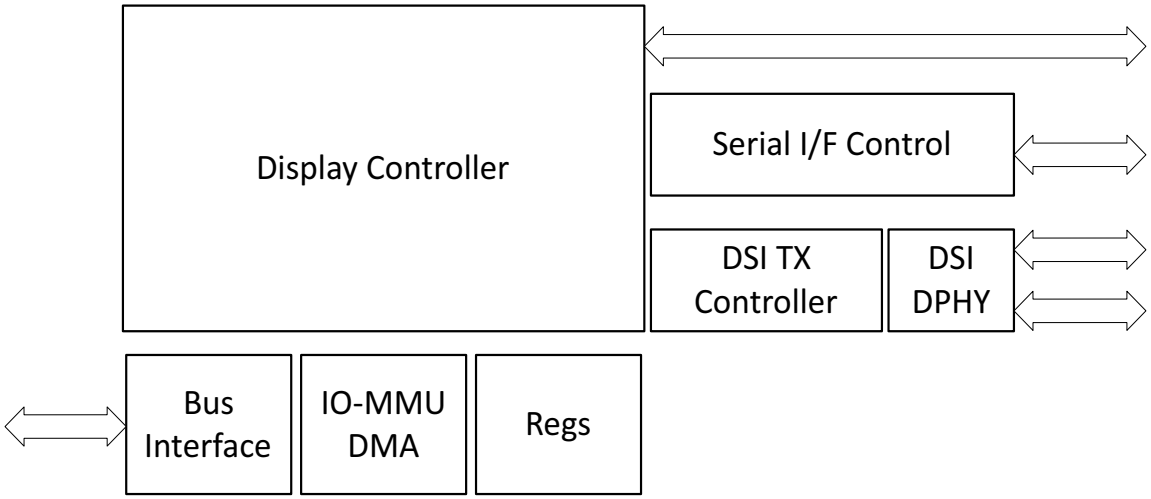

Figure 46. Block Diagram of the Display Subsystem

23.1 Features

The Apollo510 Lite SoC's Display Subsystem contains several smart tools and functionalities to compose multiple graphics by improving image quality and contributing significantly to the reduction of the SoC power consumption. The Display Controller supports composition features and a wide range of display interfaces and advanced proprietary frame-buffer compression technology. The core is designed to reduce the workload of the Graphics Processing Unit (GPU) or the host processor (CPU) in GPU-less systems, and minimize the memory bandwidth.

The Display Subsystem is represented by the block diagram shown in Figure 46. Its key features include the following:

- Supports up to 480 x 480 resolution at a frame rate of 60 fps[1]
- Up to 32-bit color
- Configurable stride/pitch enabling panning and clipping
- Single layer
- Multiple Input Surface formats
  - RGBX8888, XRGB8888 (32-bit)
  - RGB888 (24-bit)
  - RGBX4444, XRGB4444, RGBX5551, RGB565 (16-bit)
  - RGBX2222, XRGB2222, RGB332, LUT8, Grayscale (8-bit)
- Display Interfaces
  - Parallel RGB
  - MIPI DBI-Type B and DBI-Type C (Display Bus Interface)
  -
  - JDI
  - Serial formats 3-,4-beat and two phase serial 12-bit RGB
  - 3-4 Wire SPI (Serial Peripheral Interface) bus
  - DualSPI (Dual Serial Peripheral Interface) bus

1. Resulting frame rate at any particular resolution depends upon display interface speed, bus-fabric bandwidth and complexity of the graphics assets and related operations. Typically a resolution of 480 x 480 at 60 frames/second can be supported for most applications.

  - QuadSPI (Quad Serial Peripheral Interface) bus
- Programmable HSYNC, VSYNC, DE, pixel clock polarity
- Compressed frame buffer and frame buffer decompression support:
  - 4-bit
  - 6-bit (with/without Alpha)
  - 12-bit (with/without Alpha)
- Adaptive sync
- Adaptive brightness
- Powerful composition
- Programmable size, offset and format per layer
- Programmable stride/pitch enabling panning and clipping
- Palette
- Global gamma correction
- Dithering for better results on 18-bit displays
- Programmable event interrupt
- Smart DMA support

NOTE

The DSI's D1N/D1P data lane are not offered on the WLCSP package.

NOTE

24-bit, 16-bit and 8-bit color formats work only when the frame buffer resolution is set to a multiple of 4, as is the case for the startX and startY coordinates for all TSC color formats. If the panel resolution is not a multiple of 4, then the frame buffer should be sized slightly larger than the panel resolution to make it a multiple of 4.

Since the frame buffer size is just the input of each layer, the start position of the layer as the output to the panel can be any desired value. And since it is just the frame buffer that must be larger, the desired output resolution is not restricted (i.e., can be a partial frame output or full frame of resolution that is less than the frame buffer size).

NOTE

The DPI-2 display interface is not offered on the Apollo510 Lite SoC.

NOTE

The Parallel RGB and DBI-Type B display interfaces are not offered on the WLCSP package.

23.2 Functional Overview

The Display Subsystem offers flexibility for system designers to select the number of layers, functionality of composition modules and processing methods tailored to their requirements. This section provides a high-level description of the main functions, the proprietary TSC™ compression/decompression, the supported color formats, and the display format interfaces.

23.2.1 Display Controller Functionality

The Display Controller is a dedicated hardware block allowing the offload of display interface and control functions. The configuration register file controls the operation of the display controller. Timing parameters are programmable and data are fetched for each layer by a dedicated DMA engine. Additional functions include:

- Gamma adjustment
- Dithering application

23.2.1.1 Display Controller Clocking

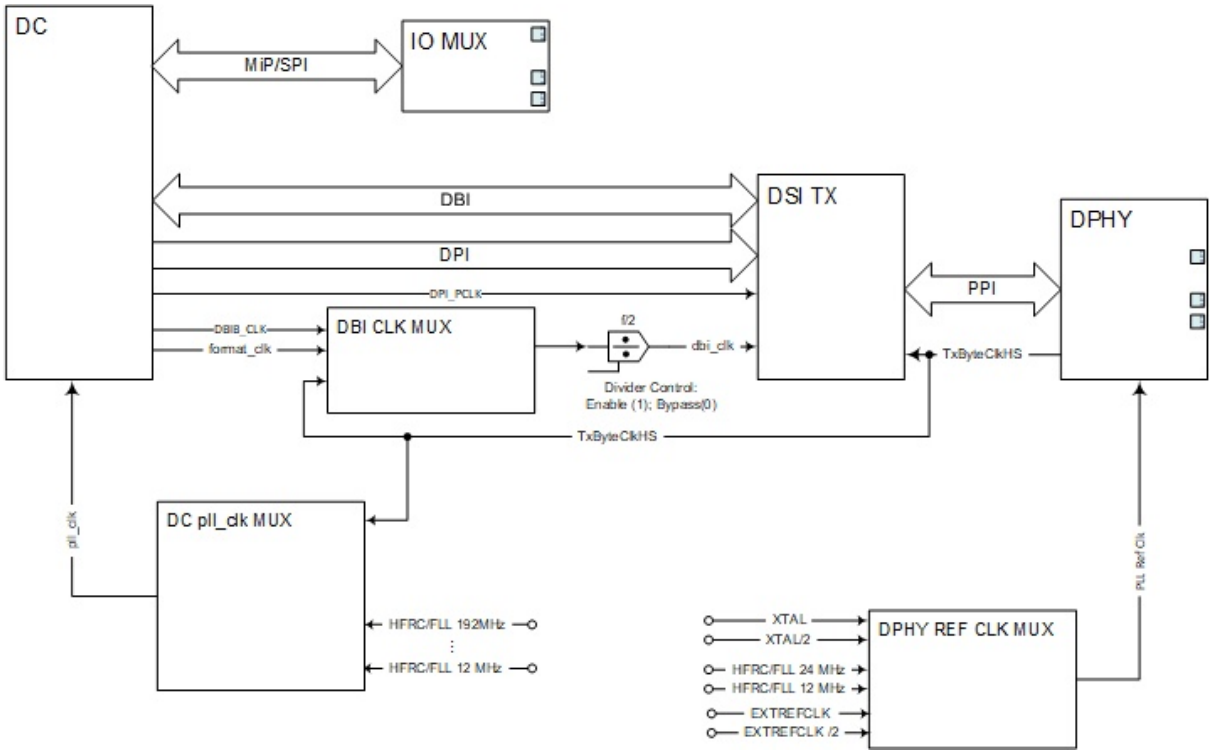

Figure 47. Display Controller Clocking Block Diagram

23.2.1.2 Video Timing Generator

The Display Controller can be configured to continuously refresh the display unit from the display buffer while the GPU optionally accesses the memory. The refresh rate, resolution and color depth of the display determine the parameters of the display controller.

The Video Timing Generator is designed to be easily programmed using timing information in the same format as X11 Modeline definitions.

23.2.1.3 Palette/Gamma Correction

The Display Controller supports palette color mapping and gamma correction.

23.2.1.4 Dithering

Dithering is the process of degrading the color image with a method that tries to produce better results than information truncation. Dithering is used to create the illusion of “color depth” in images with a limited color palette. In a dithered image, colors that are not available in the palette are approximated by a diffusion of colored pixels from within the available palette. The human eye perceives the diffusion as a mixture of the colors within it.

23.2.2 Display Serial Interface (DSI) Controller

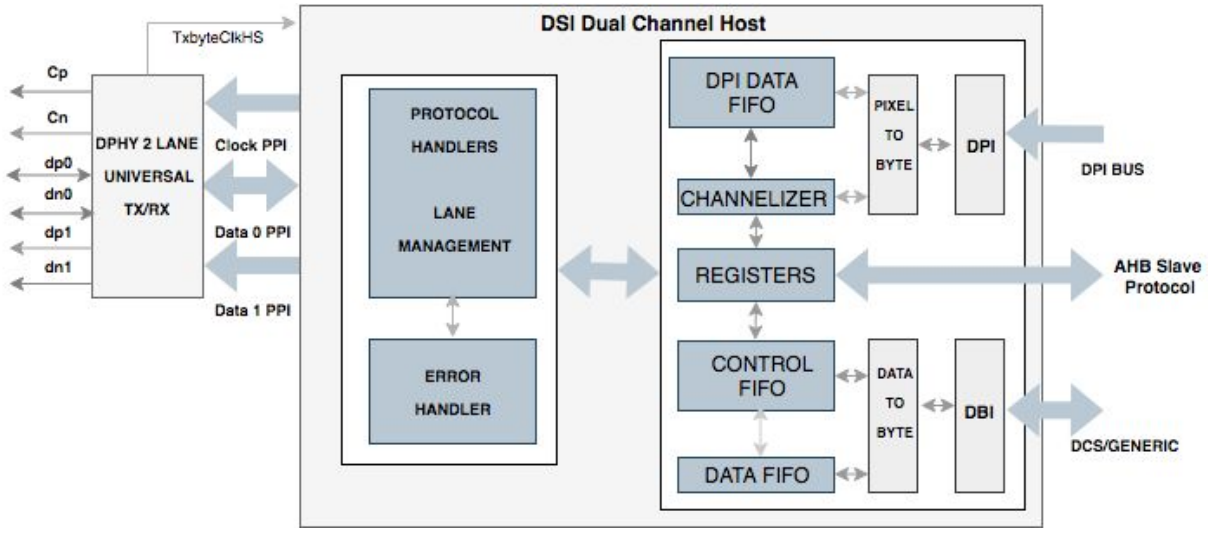

Figure 48. DSI Controller Block Diagram

23.2.2.1 DSI Features

The DSI on the Apollo510 Lite SoC supports the features listed below.

- Standard D-PHY transceiver compliant to MIPI Specification
- Type1 display architecture in command mode
- Can be programmed to support command mode in single channel mode
- DCS/Generic read and write commands
- Low power data transfer for DCS or DBI
- Pixel formats of types:
  - 16 bpp [RGB565]
  - 18 bpp [RGB666] and [Loosely packed RGB666]
  - 24 bpp [RGB888]
- Recovery from contention
- Timers and recovery schemes to come out of mode fault errors
- Watchdog timers to monitor D-PHY activity:
  - in low power mode
  - in high speed mode
  - during turn-around
- Interrupts to report protocol errors and expiry of timers
- Programmable device initialization timers
- Programmable maximum return packet size command
- One or two PHY data lanes
- DBI interface for DCS commands and data transfer
- Data lane switching to low power mode during idle time
- Signals tearing effect
- Ultra low power mode switching
- Bus turn-around
- EOT disabling capacity to suit backward compatible displays
- Clock stop enabling feature during idle time
- Supported display resolutions:
  - QCIF

- QVGA
- CIF
- VGA

The DSI is compliant with the following standards:

- DSI MIPI specification for Display Serial Interface (Version 1.3.1)
- D-PHY standard MIPI specification (Version 1.2)
- MIPI Alliance Standard for Display Bus Interface version 2.0 0
- MIPI Alliance Standard for Display Command Set Version 1.02

23.2.2.2 Functional Overview

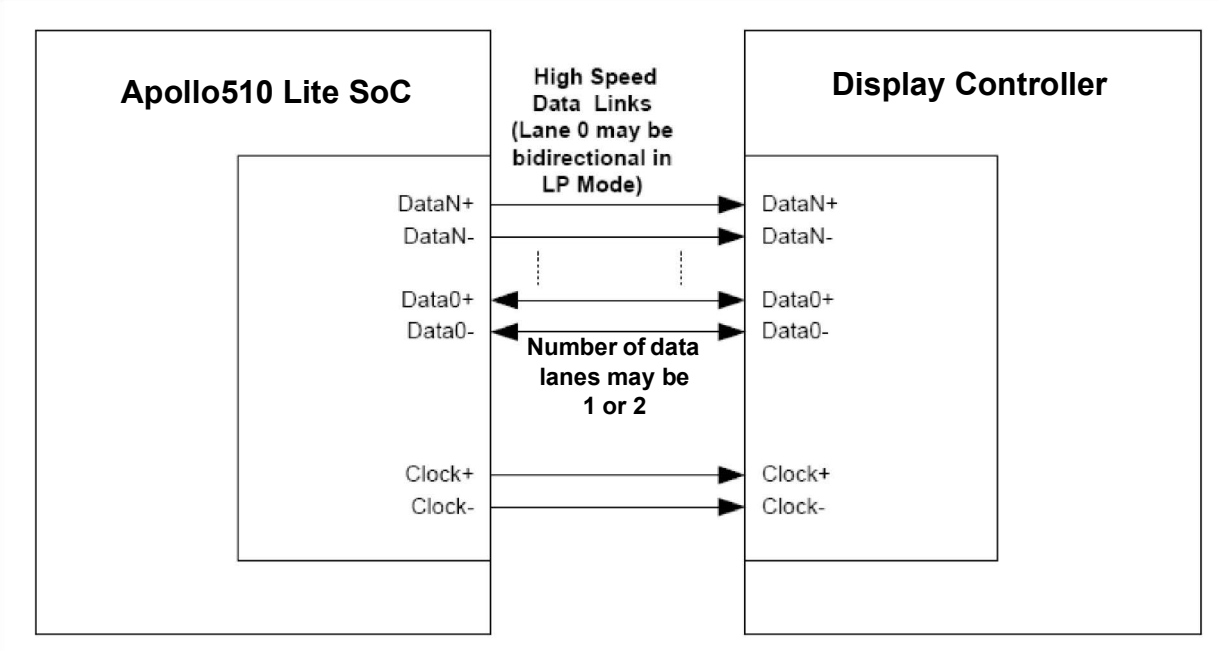

Figure 49. Display Serial Interface Bus with DSI Devices

The Display Serial Interface bus (DSI) on the Apollo510 Lite SoC is a type of serial bus that enables transfer of data between a transmitter device and a receiver device. The DSI device has a point-to-point connection with DSI devices via D-PHYs as shown in Figure 49.

The DSI module is configured to specify the interface and provide a connection between the MCU and a peripheral such as a display module. It is built on existing MIPI Alliance standards by adopting pixel formats, controlling pins and a command set specified in DBI-Type B and DCS standards.

Please refer to the DSI registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

The D-PHY's data lane signals are transferred point-to-point as differential signals using two signal lines and a clock lane. There are two signaling modes: high speed mode that operates at a rate of 768 Mbps per lane (1.536 Gbps total) and a low power mode (LP) that operates at a lower transfer rate of 10 Mbps. The mode is set to a low power mode and a stop state at start up / power up. Depending on the desired data transfer type, the lanes switch between high and low power modes. High speed data transfer is unidirectional and data transfer at low speed can be unidirectional or bidirectional.

DSI devices operate in a layered fashion. There are 4 layers identified both at receiver and transmitter ends. Figure 50 shows the layers in the DSI data transfer model.

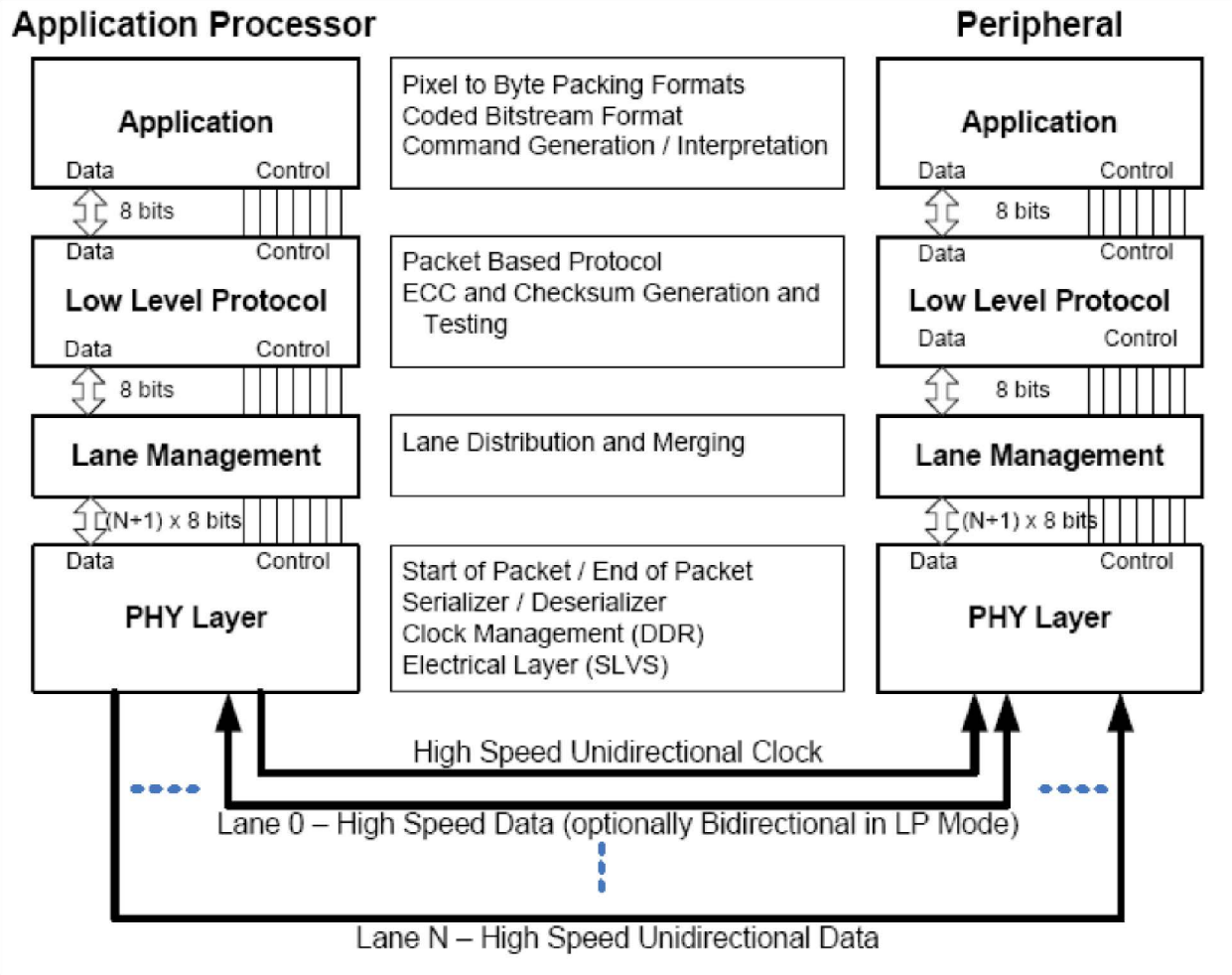

Figure 50. Layers in the DSI Data Transfer Model

PHY Layer: An embedded electrical layer that sends and detects start-of-packet and end-of-packet signaling on the data lanes. It has a serializer and deserializer unit to dialogue with the PPI / lane management unit. It also has clock divider unit to source and receive clock during different modes of operation.

PPI / Lane Management Unit: This layer does the lane buffering and distributes the data in the lanes as programmed in a round robin manner and also merges them to stream line to the LLP/ PLI unit.

PLI / Low Level Protocol Unit: This layer packetizes as well as depacketizes the data with respect to channels, frames, colors and line formats. There is an ECC generator and corrector unit to recover the data free from errors in the packet headers. It has a CRC checker or CRC generator unit to pack the payload data with CRC checksum bits for payload data protections.

Application: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module.

23.2.2.3 Hardware Design Guidelines

The following sub-sections provide design guidelines for the use of the Apollo510 Lite SoC's DSI PHY.

23.2.2.3.1 System Power Sequencing for DSI TX Interface

The following sub-sections cover the DSI TX interface (D-PHY) and addresses the proper power sequence which includes powering the VDD18 supply. Refer to the Recommended Operating Conditions section in the Electricals for VDD18 supply voltage specifications.

23.2.2.3.1.1 DSI PHY Power Tree

The recommended power tree for this configuration is as follows: VDD18 is powered by LDO rails with output discharge and ON/OFF control over I^2C or GPIO.

The following power-on (default) state is allowed: VDD18 is OFF.

23.2.2.3.1.2 DSI TX Initialization and Shutdown Sequences

Please refer to the AmbiqSuite's HAL functions (i.e., am_hal_dsi.c) for DSI PHY initialization, shut-down and other procedures.

23.3 Additional Information

Please refer to the Display Controller and DSI registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

24. Graphics Processing Unit (GPU)

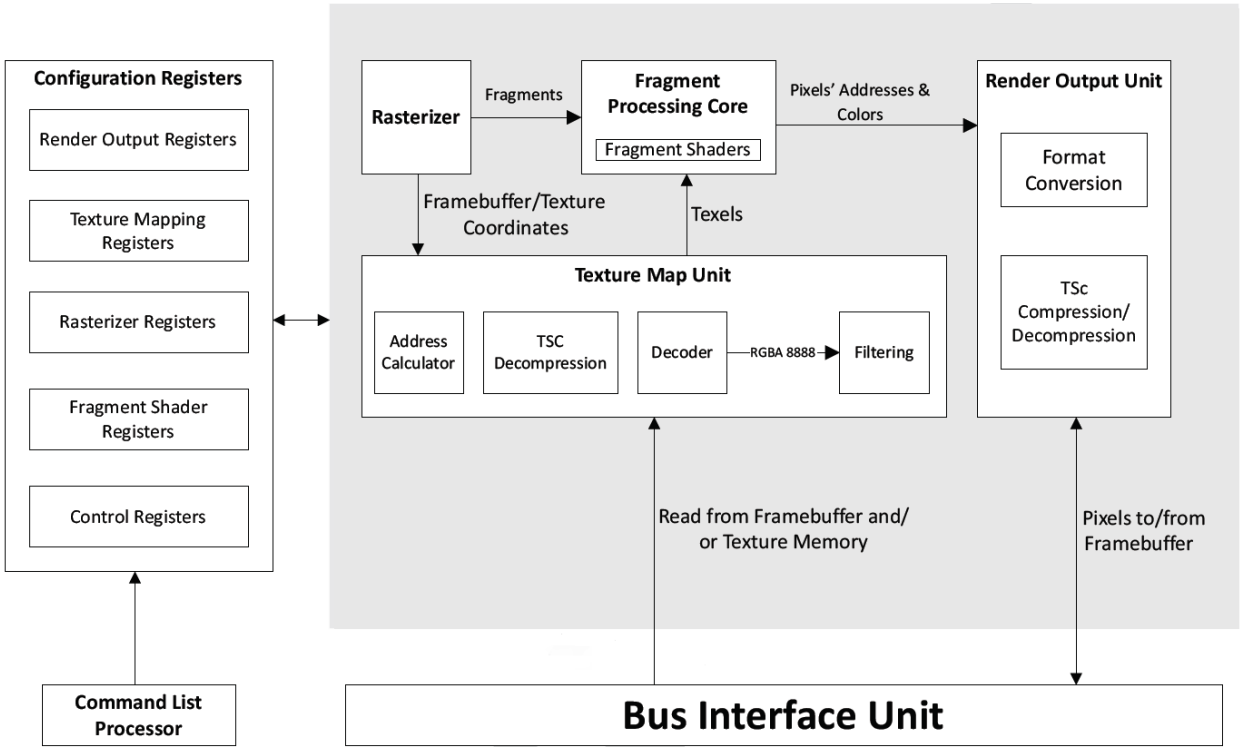

Figure 51. GPU Block Diagram

24.1 Features

The GPU Module is depicted in Figure 51. The Graphics Subsystem provides the following features:

- Fully programmable VLIW-based engine
- Fixed point functional units
- Command list based DMAs to minimize CPU overhead
- Compression schemes:
  - 4-bit
  - 6-bit (with/without Alpha)
  - 12-bit (with/without Alpha)
- 2.5D drawing
  - Pixel / Line drawing
  - Filled rectangles
  - Triangles (Gouraud Shaded)
  - Quadrilateral
- Blit support
  - Rotation
  - Mirroring
  - Stretch (independently on x and y axis)
  - Source and/or destination color keying
  - Format conversions
- Color formats
  - 32/24/16/8 bit with or without Alpha
  - Grayscale

  - RGB
- Full Alpha blending
  - Programmable blending modes
  - Source/Destination color keying
- Anti-Aliasing support
- Dithering support
- Image transformation
  - 3D Perspective Correct Projections
  - Texture mapping
    - Point sampling
    - Bilinear filtering
- Vector Graphics (VG) supported by dedicated hardware accelerator
- Configurable burst length
- Radial/Conical fill
- TrueType Font (TTF)
- Dedicated hardware to support the following:
  - Vertex Transformation
  - Bezier Tessellation
  - Bezier Draw

24.2 Functional Overview

The GPU on the Apollo510 Lite SoC brings high quality graphics for user interfaces in a very small power budget. The GPU supports entry level IoT platforms, wearable and embedded devices with low cost and ultra-low power requirements and provides fluid graphics experience for a wide range of applications. Developers are able to create compelling Graphical User Interfaces (GUIs) and software applications with ultra-long battery life at a significantly lower cost for power-memory-area constrained IoT devices.

24.3 Additional Information

Please refer to the GPU registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

25. PDM-to-PCM Converter Module (PDM)

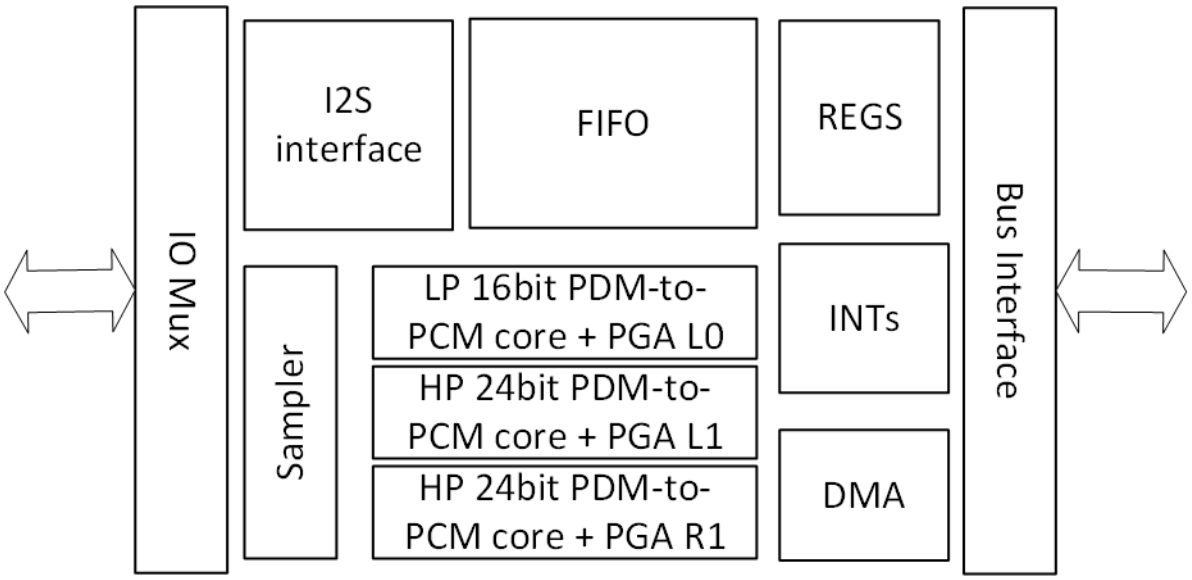

Figure 52. PDM Block Diagram

25.1 Features

The PDM-to-PCM Converter Module (PDM) includes features shown in Figure 52 and listed below.

- Support Stereo/Mono Dual Mode PDM-to-PCM Conversion
- 1-Bit PDM (pulse-density modulated) Input
- 16-Bit Low-Power (LP) Mono Mode Conversion
- 24-Bit High-Performance (HP) Mono/Stereo Mode Conversion
- On-the-Fly Dual Mode Switching
- Programmable Performance Modes
- Digital Microphone Clock
  - 400 kHz, 512 kHz, 768 kHz, 800 kHz (LP Mode)
  - 1.024 MHz, 2.048 MHz, 3.072 MHz, (HP Mode)
- PCM Sampling Rates”
  - 8 kHz, 16 kHz (LP Mode)
  - 8 kHz, 16 kHz, 24 kHz, 32 kHz, 48 kHz (HP Mode)
- Decimation Rate: 64X (typ)
- PGA Gain: -12 dB ~ + 33 dB, 3 dB/step (LP Mode); -12 dB ~ +34.5 dB, 1.5 dB/step (HP Mode)
- I^2S Subordinate Interface Pass-Through Transfer in LP Mode II

25.2 Functional Overview

The Apollo510 Lite SoC supports 1x stereo PDM controller. The PDM controller features low power stereo/ mono PDM-to-PCM converter with register programming.

The PDM controller operates in stereo or mono configuration and can operate in low power (LP - mono only) or high precision (HP) operating mode. In stereo mode, the controller converts 1-bit stereo pulse-density modulated (PDM) bit stream data from external digital microphones into 24-bit (16-bit in LP mode)

pulse-code modulated (PCM) data for base-band processing. In default operation, the PDM data sampled on the rising-edge of digital microphone clock is assumed to be left channel input, while data on the falling-edge is assumed to be right channel input. Optional channel swap is available through register setting. In mono mode, only the left channel PCM output is valid while the right channel output is zero (no toggling).

The PDM-to-PCM converter typically supports a data sampling rate of 16 kHz for voice applications. It is capable of supporting output sampling rates (Fs) of 8, 16, 24, 32 and 48 kHz at different manager clock conditions. After input sampling, the PDM data bits are fed into digital filters for data conversion and gain amplification.

DMA jobs may be ping-pong processed to allow software to pre-process and/or post-process one DMA job while hardware is processing another DMA job.

25.3 Additional Information

Please refer to the PDM registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

26. Inter-IC Sound (I^2S)

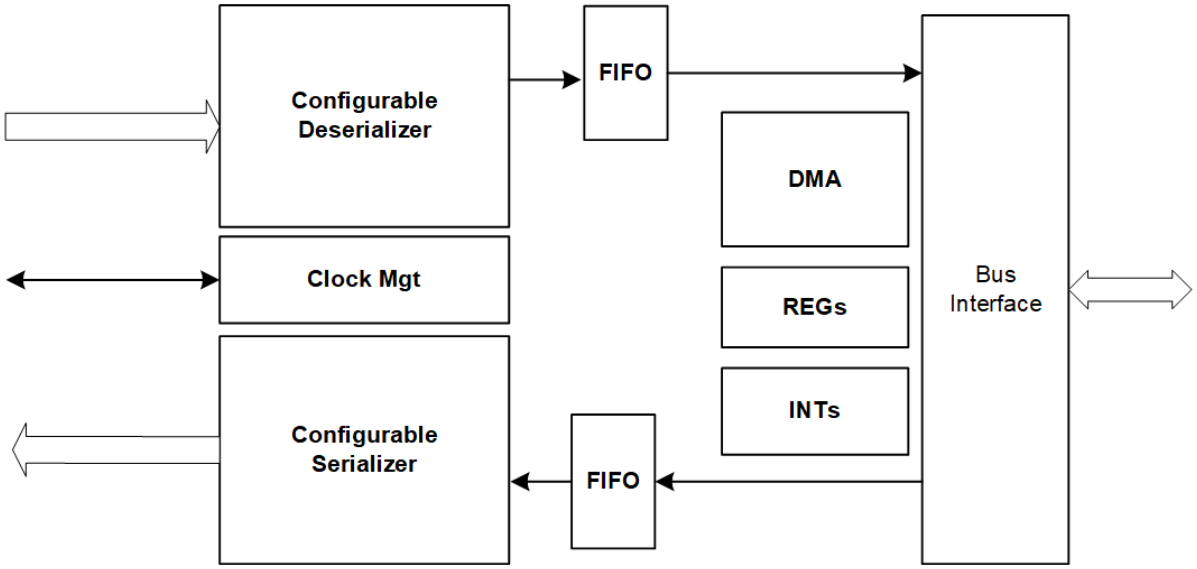

Figure 53. I^2S Block Diagram

26.1 Features

The Inter-IC Sound (I^2S) module includes features shown in Figure 53 and listed below.

- Inter-IC audio streaming interface
- Modes
  - I^2S Philips mode
  - I^2S right-justified and left-justified serial audio format modes
  - Time Division Multiplexing (TDM) mode
- Audio sample sizes of 8, 16, 24 and 32 bit
  - TDM has tremendous flexibility for framing and bit width
- 1x full-duplex I^2S instance
- Manager and subordinate
- 1 to 8 Channel TDM interface
- Sixty-four word (32-bits each) Receive FIFO
- Sixty-four word (32-bits each) Transmit FIFO

26.2 Functional Overview

The Apollo510 Lite SoC supports an I^2S controller as manager or subordinate, and full duplex. Various modes and sample rates are supported to provide flexible audio data processing. DMA is supported to enable efficient transfer of data to/from SRAM.

26.3 Additional Information

Please refer to the I^2S registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

27. Voltage Regulator Module

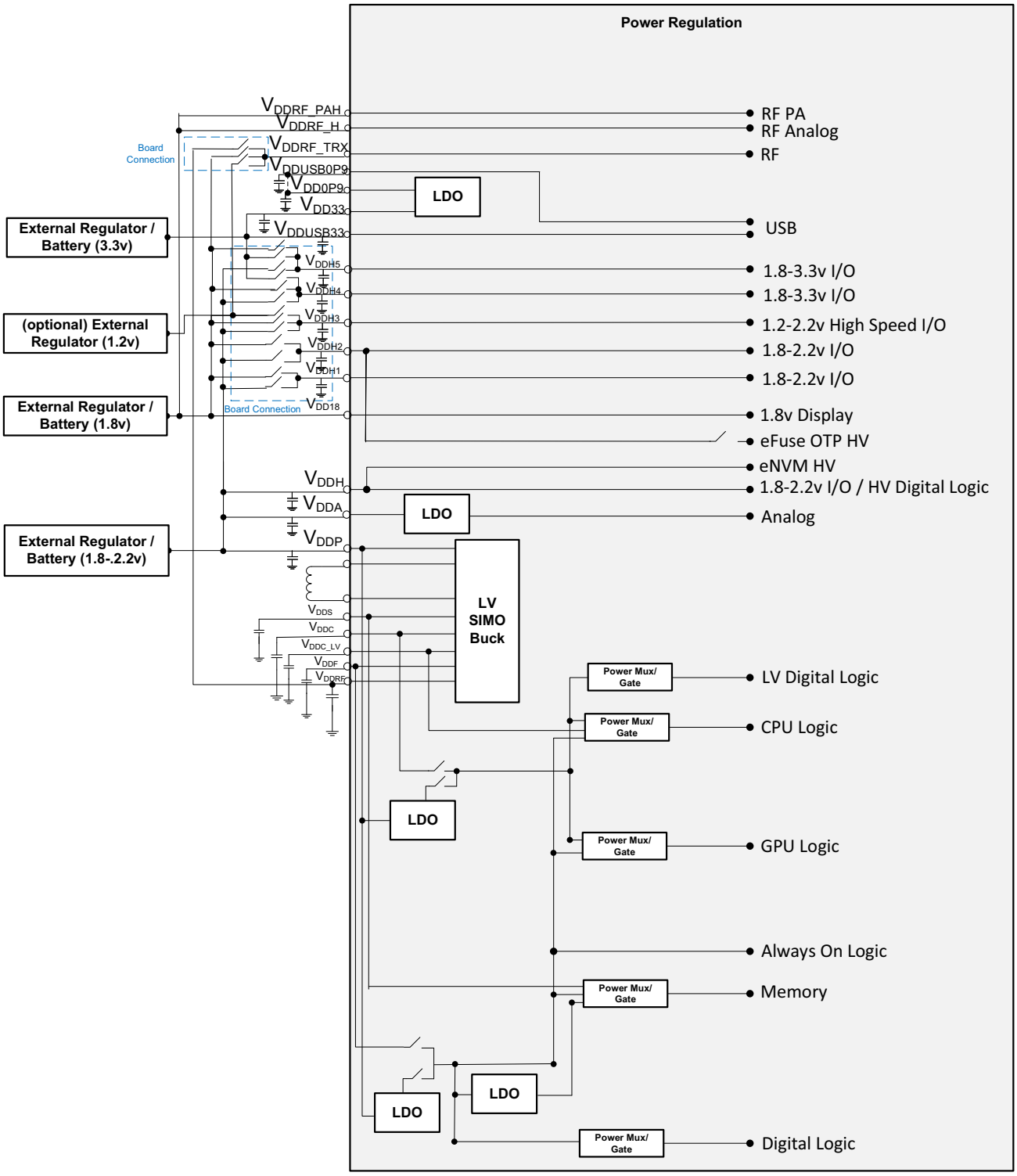

Figure 54. Block Diagram for Voltage Supplies and Regulation on Apollo510 Lite SoC

27.1 Features

The voltage supplies and regulation subsystem includes features shown in Figure 54 and listed below.

- Down-converts and efficiently regulates the VDD supply voltage
- Optimized for low power environments
- Includes single-inductor/multiple-output SIMO Buck with ultra-low quiescent current
- SIMO Buck sources primary supplies for the core and memory domains
- Prevents drop out of regulated voltages from the SIMO Buck
- Enters efficient ultra-low power mode automatically based on active system load current
- Low-dropout (LDO) linear regulator

27.2 Functional Overview

The Voltage Regulator Module on the Apollo510 Lite SoC down-converts and regulates the supply voltage, VDD, with extremely high efficiency. The SIMO Buck, which is a single-inductor/multiple-output design enabled via software, sources the primary supplies for the core and memory domains. It enables down-conversion from the power supply input (e.g., a battery or external regulator) at more than 80% efficiency. With ultra-low quiescent current, the SIMO Buck Converter is optimized for low power environments.

Upon enabling the SIMO Buck, it will be powered up and stabilized through hardware control. The SIMO Buck has an efficient ultra-low power mode that is entered automatically via hardware control based on active load current of the system. There is also a zero-length detect circuit to ensure the regulated voltages from the SIMO Buck do not drop out.

The SIMO Buck Converter and LDO of the Voltage Regulator Module are tightly coupled to the various low power modes in the Apollo510 Lite SoC. When the device enters deep sleep mode, the Buck Converter switches into a low power mode to provide very high efficiency at low quiescent current.

NOTE
The falling slew rate of a supply cannot exceed 2 kV/s. Doing so will cause indeterminate device behavior. In addition, I/O on rails should not exceed VDDHn+0.3V before the rail in question exceeds VDDHn_min, as it may cause indeterminate behavior.

27.3 Additional Information

Please refer to the voltage regulation and control registers in the MCUCTRL and PWRCTRL registers of the Apollo510 Lite SoC register set. The register set is delivered as part of the AmbiqSuite SDK.

28. Apollo510 Lite Series SoCs Package Pins

28.1 Pin Configuration

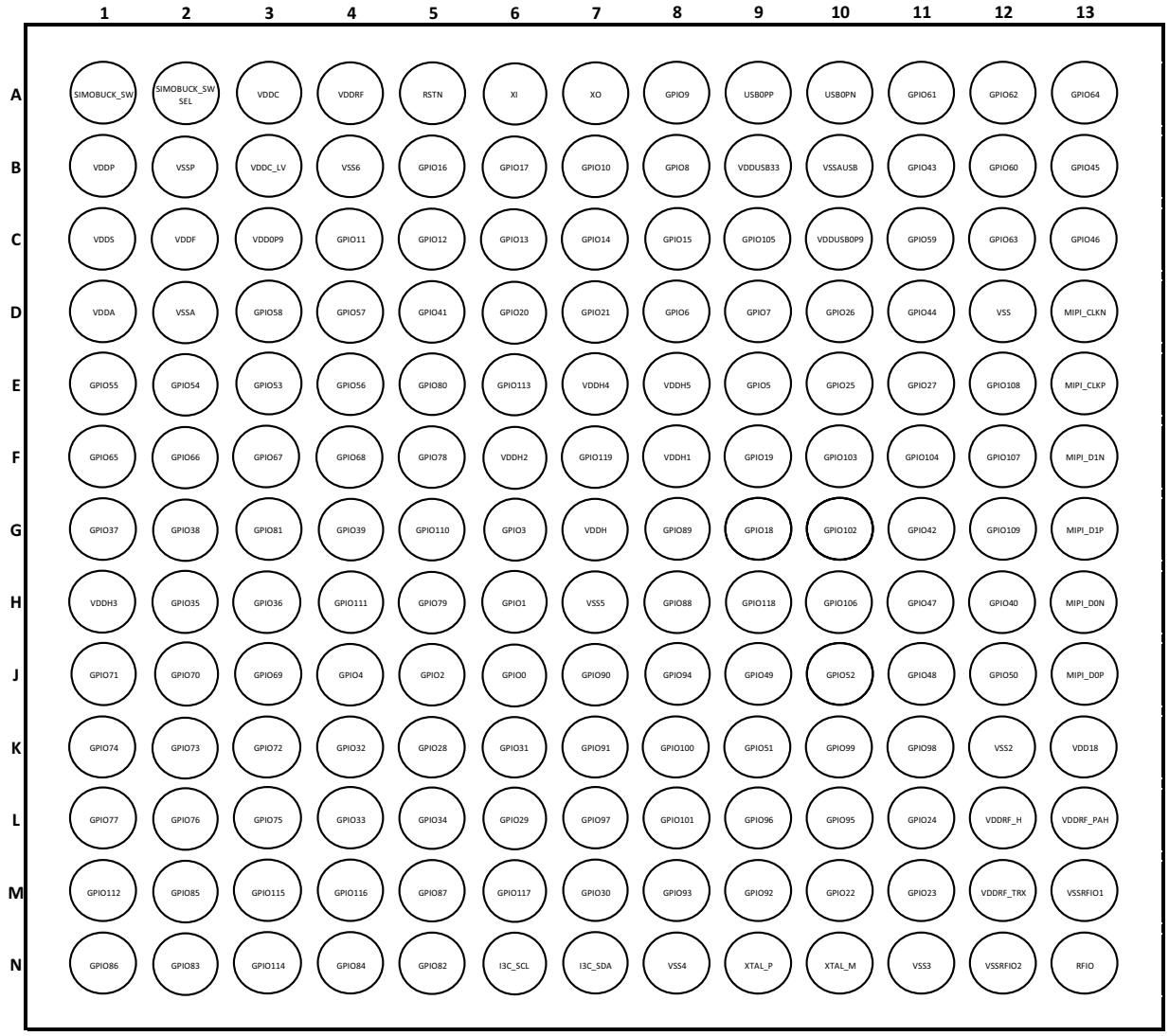

Figure 55. Apollo510 Lite Series BGA Pin Configuration Diagram - Top View

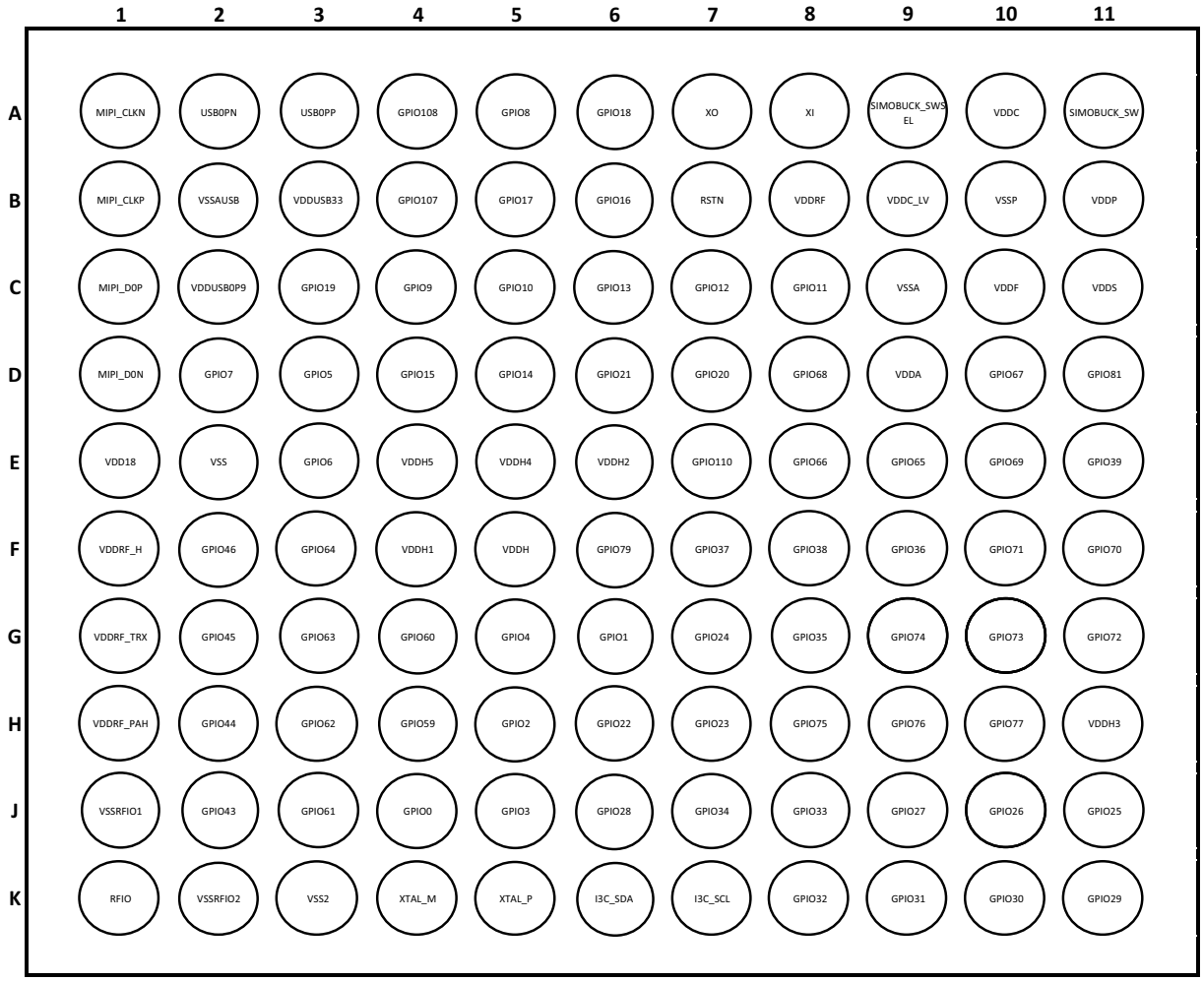

Figure 56. Apollo510 Lite Series WLCSP Pin Configuration Diagram - Top View

28.2 Pin Connections

The following table lists the external pins of the Apollo510 Lite Series SoCs and their available functions.

> NOTE
>
> The IOSFD module supports only the SPI interface. All function selection options in the below Pin List and Function Table related to IOSFD I2C interface should be ignored and not selected.

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K13	E1	-	-	VDD18	VDD supply for MIPI PHY	Power
A10	A2	-	-	USB0PN	The differential input/output signals of the PHY that support multiple modes. Depending on mode of operation they are either signaling 3.3V or 800mV differential.	Power
A9	A3	-	-	USB0PP	The differential input/output signals of the PHY that support multiple modes. Depending on mode of operation they are either signaling 3.3V or 800mV differential.	Power
D1	D9	-	-	VDDA	Analog voltage supply	Power
N11	-	-	-	VSS3	VSSRF ground	Ground
A3	A10	-	-	VDDC	Core Buck converter VOUT	Power
B3	B9	-	-	VDDC_LV	Core_LV Buck converter VOUT	Power
C2	C10	-	-	VDDF	Mem Buck converter VOUT	Power
F8	F4	-	-	VDDH1	High voltage domain1 power supply	Power
H1	H11	-	-	VDDH3	High voltage domain3 power supply	Power
C3	-	-	-	VDD0P9	0.9V Supply	Power
G7	F5	-	-	VDDH	High voltage domain power supply	Power
E7	E5	-	-	VDDH4	High voltage domain4 power supply	Power
E8	E4	-	-	VDDH5	High voltage domain5 power supply	Power
B10	B2	-	-	VSSAUSB	USB PHY Analog Ground	Ground
F6	E6	-	-	VDDH2	High voltage domain2 power supply	Power
B9	B3	-	-	VDDUSB33	USB 3.3v voltage supply	Power
K12	K3	-	-	VSS2	VSSRF ground	Ground
M12	G1	-	-	VDDRF_TRX	RF subsystem nominal voltage	Analog
L13	H1	-	-	VDDRF_PAH	RF power amplifier high Voltage	Power
L12	F1	-	-	VDDRF_H	RF analog high Voltage	Power
A4	B8	-	-	VDDRF	RF Subsystem Nominal Voltage	Power
H7	-	-	-	VSS5	VSSH ground	Ground
D12	E2	-	-	VSS	Digital Ground for VDDF and pads	Ground

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
B4	-	-	-	VSS6	VSSH ground	Ground
N8	-	-	-	VSS4	VSSH ground	Ground
B1	B11	-	-	VDDP	VDD supply to I/O pads (Core)	Power
C1	C11	-	-	VDDS	SRAM high voltage supply	Power
D2	C9	-	-	VSSA	Analog Ground - Same as GNDA	Ground
B2	B10	-	-	VSSP	Ground Connection for buck regs - Same as GNDP	Ground
A6	A8	-	-	XI	32.768kHz crystal input	XT
A7	A7	-	-	XO	32.768kHz crystal output	XT
C10	C2	-	-	VDDUSB0P9	USB 0.9v analog voltage supply	Power
D13	A1	-	-	MIPI_CLKN	MIPI DPHY Clock Lane N	I/O
E13	B1	-	-	MIPI_CLKP	MIPI DPHY Clock Lane P	I/O
H13	D1	-	-	MIPI_D0N	MIPI DPHY Data Lane 0N	I/O
J13	C1	-	-	MIPI_D0P	MIPI DPHY Data Lane 0P	I/O
F13	-	-	-	MIPI_D1N	MIPI DPHY Data Lane 1N	I/O
G13	-	-	-	MIPI_D1P	MIPI DPHY Data Lane 1P	I/O
A5	B7	-	-	RSTN	External reset input (aka nRST)	Input
A1	A11	-	-	SIMOBUCK_SW	SIMO Buck converter inductor switch output	Power
A2	A9	-	-	SIMOBUCK_SWSEL	SIMO Buck converter inductor switch input	Power
N9	K5	-	-	XTAL_P	RF crystal output	XTAL_RF
N10	K4	-	-	XTAL_M	RF crystal input	XTAL_RF
M13	J1	-	-	VSSRFIO1	RF Antenna Ground	Power
N12	K2	-	-	VSSRFIO2	RF Antenna Ground	Power
N6	K7	-	-	I3C_SCL	I3C Manager clock	Open Drain Output
N7	K6	-	-	I3C_SDA	I3C Manager I/O data	Bidirectional Open Drain
N13	K1	-	-	RFIO	RF Antenna	Analog

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J6	J4	0	0	SWTRACECLK	Serial Wire Debug Trace Clock	Output
			1	SLFDSCK	SPI Slave Full Duplex clock	Input
			2	DISP_QSPI_D0	Display SPI Data0	Bidirectional
			3	GPIO0	General purpose I/O	I/O
			4	DISP_SPI_SD	Display SPI Data Out	Bidirectional
			5	DISP_SPI_SDO	Display SPI Data Out	Output
			6	CT0	Timer/counter 0	Output
			7	NCE0	IOMSTR N Chip Select 0	Output
			9	-	-	-
			10	-	-	-
			12	SLFDSCL	I2C Slave Full Duplex clock	Input
			13	DISP_QSPI_D0_OUT	Display SPI Data0	Output
H6	G6	1	0	SWTRACE0	Serial Wire Debug Trace Output 0	Output
			1	SLFDMOSI	SPI Slave Full Duplex input data	Input
			2	DISP_QSPI_D1	Display SPI Data1	Output
			3	GPIO1	General purpose I/O	I/O
			4	DISP_SPI_DCX	Display SPI DCx	Output
			5	-	-	-
			6	CT1	Timer/counter 1	Output
			7	NCE1	IOMSTR N Chip Select 1	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	SLFDSDAWIR3	I2C Slave Full Duplex I/O data (I2C) 3 Wire Data (SPI)	Bidirectional Open Drain
			13	-	-	-
J5	H5	2	0	SWTRACE1	Serial Wire Debug Trace Output 1	Output
			1	SLFDMISO	SPI Slave Full Duplex output data	Output
			2	DISP_QSPI_SCK	Display SPI CLK	Output
			3	GPIO2	General purpose I/O	I/O
			4	DISP_SPI_SCK	Display SPI Clock	Output
			5	-	-	-
			6	CT2	Timer/counter 2	Output
			7	NCE2	IOMSTR N Chip Select 2	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	XT_EXT	External XT Clock	Input
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G6	J5	3	0	SWTRACE2	Serial Wire Debug Trace Output 2	Output
			1	SLFDnCE	SPI Slave Full Duplex chip enable	Input
			2	DISP_QSPI_D2	Display SPI Data2	Output
			3	GPIO3	General purpose I/O	I/O
			4	DISP_SPI_SDI	Display SPI Data IN	input
			5	-	-	-
			6	CT3	Timer/counter 3	Output
			7	NCE3	IOMSTR N Chip Select 3	Output
			9	-	-	-
			10	-	-	-
			12	-	-	-
			13	-	-	-
J4	G5	4	0	SWTRACE3	Serial Wire Debug Trace Output 3	Output
			1	SLFDINT	Configurable Slave Interrupt	Output
			2	DISP_QSPI_D3	Display SPI Data3	Output
			3	GPIO4	General purpose I/O	I/O
			4	DISP_SPI_RST	Display SPI Reset	Output
			5	-	-	-
			6	CT4	Timer/counter 4	Output
			7	NCE4	IOMSTR N Chip Select 4	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
E9	D3	5	0	M0SCL	I2C Manager 0 clock	Open Drain Output
			1	M0SCK	SPI Manager 0 clock	Output
			2	PDMI2S0_SDOUT	PDMI2S0 Data output	Output
			3	GPIO5	General purpose I/O	I/O
			4	-	-	-
			5	32KHzXT	32kHZ from analog	Output
			6	CT5	Timer/counter 5	Output
			7	NCE5	IOMSTR N Chip Select 5	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	I2S0_SDOUT	I2S0 Data output	Output
			13	I2S0_DATA	I2S0 Data	Bidirectional

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
D8	E3	6	0	M0SDAWIR3	I2C Manager 0 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
			1	M0MOSI	SPI Manager 0 output data	Output
			2	PDMI2S0_WS	PDMI2S0 L/R clock	Bidirectional
			3	GPIO6	General purpose I/O	I/O
			4	CLKOUT	Oscillator output clock	Output
			5	-	-	-
			6	CT6	Timer/counter 6	Output
			7	NCE6	IOMSTR N Chip Select 6	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	I2S0_WS	I2S0 L/R clock	Bidirectional
			13	-	-	-
D9	D2	7	0	M0MISO	SPI Manager 0 input data	Input
			1	VCMPO	Output of the voltage comparator signal	-
			2	-	-	-
			3	GPIO7	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT7	Timer/counter 7	Output
			7	NCE7	IOMSTR N Chip Select 7	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	I2S0_SDIN	I2S0 Data input	Input
			13	-	-	-
B8	A5	8	0	CMPRF1	Comparator reference 1	Input
			1	M1SCL	I2C Manager 1 clock	Open Drain Output
			2	M1SCK	SPI Manager 1 clock	Output
			3	GPIO8	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT8	Timer/counter 8	Output
			7	NCE8	IOMSTR N Chip Select 8	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
A8	C4	9	0	CMPRF0	Comparator reference 0	Input
			1	M1SDAWIR3	I2C Manager 1 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
			2	M1MOSI	SPI Manager 1 output data	Output
			3	GPIO9	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT9	Timer/counter 9	Output
			7	NCE9	IOMSTR N Chip Select 9	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
B7	C5	10	0	CMPIN0	Voltage comparator input 0	Input
			1	M1MISO	SPI Manager 1 input data	Input
			2	PDMI2S0_CLK	PDMI2S0 Bit clock	Bidirectional
			3	GPIO10	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT10	Timer/counter 10	Output
			7	NCE10	IOMSTR N Chip Select 10	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	I2S0_CLK	I2S0 Bit clock	Bidirectional
			13	-	-	-
C4	C8	11	0	CMPIN1	Voltage comparator input 1	Input
			1	-	-	-
			2	PDMI2S0_CLK	PDMI2S0 Bit clock	Bidirectional
			3	GPIO11	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT11	Timer/counter 11	Output
			7	NCE11	IOMSTR N Chip Select 11	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	I2S0_CLK	I2S0 Bit clock	Bidirectional
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
C5	C7	12	0	ADCSE7	Analog to Digital Converter SE IN7	Input
			1	-	-	-
			2	PDMI2S0_WS	PDMI2S0 L/R clock	Bidirectional
			3	GPIO12	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	CMPRF2	Comparator reference 2	Input
			6	CT12	Timer/counter 12	Output
			7	NCE12	IOMSTR N Chip Select 12	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	I2S0_WS	I2S0 L/R clock	Bidirectional
			13	-	-	-
C6	C6	13	0	ADCSE6	Analog to Digital Converter SE IN6	Input
			1	-	-	-
			2	PDMI2S0_SDOUT	PDMI2S0 Data output	Output
			3	GPIO13	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT13	Timer/counter 13	Output
			7	NCE13	IOMSTR N Chip Select 13	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	I2S0_SDOUT	I2S0 Data output	Output
			13	I2S0_DATA	I2S0 Data	Bidirectional
C7	D5	14	0	ADCSE5	Analog to Digital Converter SE IN5	Input
			1	-	-	-
			2	-	-	-
			3	GPIO14	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT14	Timer/counter 14	Output
			7	NCE14	IOMSTR N Chip Select 14	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	I2S0_SDIN	I2S0 Data input	Input
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
C8	D4	15	0	ADCSE4	Analog to Digital Converter SE IN4	Input
			1	REFCLK_EXT	External Reference Clock	Input
			2	-	-	-
			3	GPIO15	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT15	Timer/counter 15	Output
			7	NCE15	IOMSTR N Chip Select 15	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
B5	B6	16	0	ADCSE3	Analog to Digital Converter SE IN3	Input
			1	-	-	-
			2	-	-	-
			3	GPIO16	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT16	Timer/counter 16	Output
			7	NCE16	IOMSTR N Chip Select 16	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
B6	B5	17	0	ADCSE2	Analog to Digital Converter SE IN2	Input
			1	-	-	-
			2	-	-	-
			3	GPIO17	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT17	Timer/counter 17	Output
			7	NCE17	IOMSTR N Chip Select 17	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G9	A6	18	0	ADCSE1	Analog to Digital Converter SE IN1	Input
			1	-	-	-
			2	-	-	-
			3	GPIO18	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT18	Timer/counter 18	Output
			7	NCE18	IOMSTR N Chip Select 18	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
F9	C3	19	0	ADCSE0	Analog to Digital Converter SE IN0	Input
			1	-	-	-
			2	-	-	-
			3	GPIO19	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT19	Timer/counter 19	Output
			7	NCE19	IOMSTR N Chip Select 19	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
D6	D7	20	0	SWDCK	Software debug clock Input	Input
			1	-	-	-
			2	-	-	-
			3	GPIO20	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT20	Timer/counter 20	Output
			7	NCE20	IOMSTR N Chip Select 20	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
D7	D6	21	0	SWDIO	Software data I/O	Bidirectional 3-state
			1	-	-	-
			2	-	-	-
			3	GPIO21	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT21	Timer/counter 21	Output
			7	NCE21	IOMSTR N Chip Select 21	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
M10	H6	22	0	M5SCL	I2C Manager 5 Clk	Bidirectional Open Drain
			1	M5SCK	SPI Manager 5 Clk	Output
			2	-	-	-
			3	GPIO22	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT22	Timer/counter 22	Output
			7	NCE22	IOMSTR N Chip Select 22	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	RF_XCVR_TST0	BTDM DSP Diagnostic Test	Output
			13	-	-	-
M11	H7	23	0	M5SDAWIR3	I2C Manager 5 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
			1	M5MOSI	SPI Manager 5 data out	Output
			2	BTDM_RXEN	BTDM RX Enable	Output
			3	GPIO23	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT23	Timer/counter 23	Output
			7	NCE23	IOMSTR N Chip Select 23	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	ST_WCI_2W_RXD	BTDM DSP Diagnostic Test	Output
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
L11	G7	24	0	M5MISO	SPI Manager 5 data in	Input
			1	-	-	-
			2	BTDM_TXEN	BTDM TX Enable	Output
			3	GPIO24	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT24	Timer/counter 24	Output
			7	NCE24	IOMSTR N Chip Select 24	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	ST_WCI_1W_RXD	BTDM	Output
			13	ST_WCI_2W_TXD	BTDM	Output
E10	J11	25	0	M2SCL	I2C Manager 2 clock	Open Drain Output
			1	M2SCK	SPI Manager 2 clock	Output
			2	VCMPO	Output of the voltage comparator signal	-
			3	GPIO25	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT25	Timer/counter 25	Output
			7	NCE25	IOMSTR N Chip Select 25	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
D10	J10	26	0	M2SDAWIR3	I2C Manager 2 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
			1	M2MOSI	SPI Manager 2 output data	Output
			2	-	-	-
			3	GPIO26	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	SWTRACECTL	Serial Wire Debug Trace Control	Output
			6	CT26	Timer/counter 26	Output
			7	NCE26	IOMSTR N Chip Select 26	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
E11	J9	27	0	M2MISO	SPI Manager 2 input data	Input
			1	I2S0_MCLK	I2S0 MCLK`	Bidirectional
			2	VCMPO	Output of the voltage comparator signal	-
			3	GPIO27	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT27	Timer/counter 27	Output
			7	NCE27	IOMSTR N Chip Select 27	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
K5	J6	28	0	SWO	Serial Wire Debug	Output
			1	SWTRACECTL	Serial Wire Debug Trace Control	Output
			2	-	-	-
			3	GPIO28	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT28	Timer/counter 28	Output
			7	NCE28	IOMSTR N Chip Select 28	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
L6	K11	29	0	M3SCL	I2C Manager 3 clock	Open Drain Output
			1	M3SCK	SPI Manager 3 clock	Output
			2	-	-	-
			3	GPIO29	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT29	Timer/counter 29	Output
			7	NCE29	IOMSTR N Chip Select 29	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	I2S0_SDIN	I2S0 Data input	Input
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
M7	K10	30	0	M3SDAWIR3	I2C Manager 3 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
			1	M3MOSI	SPI Manager 3 output data	Output
			2	PDMI2S0_SDOUT	PDMI2S0 Data output	Output
			3	GPIO30	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT30	Timer/counter 30	Output
			7	NCE30	IOMSTR N Chip Select 30	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	I2S0_SDOUT	I2S0 Data output	Output
			13	I2S0_DATA	I2S0 Data	Bidirectional
K6	K9	31	0	M3MISO	SPI Manager 3 input data	Input
			1	CLKOUT	Oscillator output clock	Output
			2	PDMI2S0_WS	PDMI2S0 L/R clock	Bidirectional
			3	GPIO31	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	COEX_GRANT	Coexistence Grant	Input
			6	CT31	Timer/counter 31	Output
			7	NCE31	IOMSTR N Chip Select 31	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	I2S0_WS	I2S0 L/R clock	Bidirectional
			13	-	-	-
K4	K8	32	0	M4SCL	I2C Manager 4 Clk	Output
			1	M4SCK	SPI Manager 4 Clk	Output
			2	-	-	-
			3	GPIO32	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	COEX_REQ	Coexistence Request	Input
			6	CT32	Timer/counter 32	Output
			7	NCE32	IOMSTR N Chip Select 32	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
L4	J8	33	0	M4SDAWIR3	I2C Manager 4 I/O data (I2C) 3 Wire data (SPI)	Bidirectional Open Drain
			1	M4MOSI	SPI Manager 4 data out	Input
			2	-	-	-
			3	GPIO33	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	COEX_PRIORITY	Coexistence Priority Control	Input
			6	CT33	Timer/counter 33	Output
			7	NCE33	IOMSTR N Chip Select 33	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
L5	J7	34	0	M4MISO	SPI Manager 4 data in	Input
			1	SWO	Serial Wire Debug	Output
			2	-	-	-
			3	GPIO34	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	COEX_FREQ	Coexistence Frequency Control	Input
			6	CT34	Timer/counter 34	Output
			7	NCE34	IOMSTR N Chip Select 34	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
H2	G8	35	0	MSPI0_8	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACECLK	Serial Wire Debug Trace Clock	Output
			2	-	-	-
			3	GPIO35	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT35	Timer/counter 35	Output
			7	NCE35	IOMSTR N Chip Select 35	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
H3	F9	36	0	MSPI0_0	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE0	Serial Wire Debug Trace Output 0	Output
			2	-	-	-
			3	GPIO36	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT36	Timer/counter 36	Output
			7	NCE36	IOMSTR N Chip Select 36	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
G1	F7	37	0	MSPI0_1	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE1	Serial Wire Debug Trace Output 1	Output
			2	-	-	-
			3	GPIO37	General purpose I/O	I/O
			4	-	-	-
			5	32KHzXT	32kHZ from analog	Output
			6	CT37	Timer/counter 37	Output
			7	NCE37	IOMSTR N Chip Select 37	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
G2	F8	38	0	MSPI0_2	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE2	Serial Wire Debug Trace Output 2	Output
			2	-	-	-
			3	GPIO38	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT38	Timer/counter 38	Output
			7	NCE38	IOMSTR N Chip Select 38	Output
			9	-	-	-
			10	-	-	-
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G4	E11	39	0	MSPI0_3	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE3	Serial Wire Debug Trace Output 3	Output
			2	-	-	-
			3	GPIO39	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT39	Timer/counter 39	Output
			7	NCE39	IOMSTR N Chip Select 39	Output
			9	-	-	-
			10	-	-	-
			12	-	-	-
			13	-	-	-
H12	NC	40	0	MNCE1_0	MSPI Manager 1 nCE 0 Signal	-
			1	-	-	-
			2	-	-	-
			3	GPIO40	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT40	Timer/counter 40	Output
			7	NCE40	IOMSTR N Chip Select 40	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
D5	NC	41	0	MNCE2_0	MSPI Manager 2 nCE 0 Signal	-
			1	-	-	-
			2	-	-	-
			3	GPIO41	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT41	Timer/counter 41	Output
			7	NCE41	IOMSTR N Chip Select 41	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G11	NC	42	0	MNCE1_1	MSPI Manager 1 nCE 1 Signal	-
			1	DISP_TE	Display TE input	Input
			2	-	-	-
			3	GPIO42	General purpose I/O	I/O
			4	ST_WCI_1W_RXD	BTDM	Output
			5	ST_WCI_2W_TXD	BTDM	Output
			6	CT42	Timer/counter 42	Output
			7	NCE42	IOMSTR N Chip Select 42	Output
			9	-	-	-
			10	-	-	-
			12	BTDM_RXEN	BTDM RX Enable	Output
			13	-	-	-
B11	J2	43	0	-	-	-
			1	SDIF1_DAT4	SD/SDIO/MMC Data4 pin	I/O
			2	COEX_GRANT	Coexistence Grant	Input
			3	GPIO43	General purpose I/O	I/O
			4	PDMI2S0_SDOUT	PDMI2S0 Data output	Output
			5	-	-	-
			6	CT43	Timer/counter 43	Output
			7	NCE43	IOMSTR N Chip Select 43	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	I2S0_SDOUT	I2S0 Data output	Output
			13	I2S0_DATA	I2S0 Data	Bidirectional
D11	H2	44	0	-	-	-
			1	SDIF1_DAT5	SD/SDIO/MMC Data5 pin	I/O
			2	COEX_REQ	Coexistence Request	Input
			3	GPIO44	General purpose I/O	I/O
			4	PDMI2S0_WS	PDMI2S0 L/R clock	Bidirectional
			5	SWO	Serial Wire Debug	Output
			6	CT44	Timer/counter 44	Output
			7	NCE44	IOMSTR N Chip Select 44	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	I2S0_WS	I2S0 L/R clock	Bidirectional
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
B13	G2	45	0	-	-	-
			1	SDIF1_DAT6	SD/SDIO/MMC Data6 pin	I/O
			2	COEX_PRIORITY	Coexistence Priority Control	Input
			3	GPIO45	General purpose I/O	I/O
			4	-	-	-
			5	32KHzXT	32kHZ from analog	Output
			6	CT45	Timer/counter 45	Output
			7	NCE45	IOMSTR N Chip Select 45	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	I2S0_SDIN	I2S0 Data input	Input
			13	-	-	-
C13	F2	46	0	I2S0_MCLK	I2S0 MCLK`	Bidirectional
			1	SDIF1_DAT7	SD/SDIO/MMC Data7 pin	I/O
			2	COEX_FREQ	Coexistence Frequency Control	Input
			3	GPIO46	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT46	Timer/counter 46	Output
			7	NCE46	IOMSTR/MSPI N Chip Select 46	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
H11	NC	47	0	MSPI1_4	MSPI Manager 1 Interface Signal	I/O
			1	SWTRACECLK	Serial Wire Debug Trace Clock	Output
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO47	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT47	Timer/counter 47	Output
			7	NCE47	IOMSTR N Chip Select 47	Output
			9	-	-	-
			10	-	-	-
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J11	NC	48	0	MSPI1_0	MSPI Manager 1 Interface Signal	I/O
			1	SWTRACE0	Serial Wire Debug Trace Output 0	Output
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO48	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT48	Timer/counter 48	Output
			7	NCE48	IOMSTR N Chip Select 48	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
J9	NC	49	0	MSPI1_1	MSPI Manager 1 Interface Signal	I/O
			1	SWTRACE1	Serial Wire Debug Trace Output 1	Output
			2	-	-	-
			3	GPIO49	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT49	Timer/counter 49	Output
			7	NCE49	IOMSTR N Chip Select 49	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
J12	NC	50	0	MSPI1_2	MSPI Manager 1 Interface Signal	I/O
			1	SWTRACE2	Serial Wire Debug Trace Output 2	Output
			2	-	-	-
			3	GPIO50	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT50	Timer/counter 50	Output
			7	NCE50	IOMSTR N Chip Select 50	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K9	NC	51	0	MSPI1_3	MSPI Manager 1 Interface Signal	I/O
			1	SWTRACE3	Serial Wire Debug Trace Output 3	Output
			2	-	-	-
			3	GPIO51	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT51	Timer/counter 51	Output
			7	NCE51	IOMSTR N Chip Select 51	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
J10	NC	52	0	MSPI1_5	MSPI Manager 1 Interface Signal	I/O
			1	SWTRACECTL	Serial Wire Debug Trace Control	Output
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO52	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT52	Timer/counter 52	Output
			7	NCE52	IOMSTR/MSPI N Chip Select 52	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
E3	NC	53	0	MSPI2_8	MSPI Manager 2 Interface Signal	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO53	General purpose I/O	I/O
			4	-	-	-
			5	SWO	Serial Wire Debug	Output
			6	CT53	Timer/counter 53	Output
			7	NCE53	IOMSTR N Chip Select 53	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
E2	NC	54	0	MSPI2_0	MSPI Manager 2 Interface Signal	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO54	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT54	Timer/counter 54	Output
			7	NCE54	IOMSTR N Chip Select 54	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
E1	NC	55	0	MSPI2_1	MSPI Manager 2 Interface Signal	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO55	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT55	Timer/counter 55	Output
			7	NCE55	IOMSTR N Chip Select 55	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
E4	NC	56	0	MSPI2_2	MSPI Manager 2 Interface Signal	I/O
			1	-	-	-
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO56	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT56	Timer/counter 56	Output
			7	NCE56	IOMSTR/MSPI N Chip Select 56	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
D4	NC	57	0	MSPI2_3	MSPI Manager 2 Interface Signal	I/O
			1	-	-	-
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO57	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT57	Timer/counter 57	Output
			7	NCE57	IOMSTR/MSPI N Chip Select 57	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
D3	NC	58	0	MSPI2_9	MSPI Manager 2 Interface Signal	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO58	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT58	Timer/counter 58	Output
			7	NCE58	IOMSTR N Chip Select 58	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
C11	H4	59	0	SDIF1_DAT0	SD/SDIO/MMC Data0 pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO59	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT59	Timer/counter 59	Output
			7	NCE59	IOMSTR N Chip Select 59	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
B12	G4	60	0	SDIF1_DAT1	SD/SDIO/MMC Data1 pin	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO60	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT60	Timer/counter 60	Output
			7	NCE60	IOMSTR/MSPI N Chip Select 60	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
A11	J3	61	0	SDIF1_DAT2	SD/SDIO/MMC Data2 pin	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO61	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT61	Timer/counter 61	Output
			7	NCE61	IOMSTR N Chip Select 61	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
A12	H3	62	0	SDIF1_DAT3	SD/SDIO/MMC Data3 pin	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO62	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT62	Timer/counter 62	Output
			7	NCE62	IOMSTR N Chip Select 62	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
C12	G3	63	0	SDIF1_CLKOUT	SD/SDIO/MMC Clock to Card (CLK)	Output
			1	-	-	-
			2	-	-	-
			3	GPIO63	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT63	Timer/counter 63	Output
			7	NCE63	IOMSTR N Chip Select 63	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
A13	F3	64	0	SDIF1_CMD	SD1/SD4/MMC Command pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO64	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT64	Timer/counter 64	Output
			7	NCE64	IOMSTR N Chip Select 64	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
F1	E9	65	0	MSPI0_4	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO65	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT65	Timer/counter 65	Output
			7	NCE65	IOMSTR N Chip Select 65	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
F2	E8	66	0	MSPI0_5	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO66	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT66	Timer/counter 66	Output
			7	NCE66	IOMSTR N Chip Select 66	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
F3	D10	67	0	MSPI0_6	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO67	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT67	Timer/counter 67	Output
			7	NCE67	IOMSTR N Chip Select 67	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
F4	D8	68	0	MSPI0_7	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO68	General purpose I/O	I/O
			4	-	-	-
			5	SWO	Serial Wire Debug	Output
			6	CT68	Timer/counter 68	Output
			7	NCE68	IOMSTR N Chip Select 68	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J3	E10	69	0	MSPI0_10	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO69	General purpose I/O	I/O
			4	MSPI2_0	MSPI Manager 2 Interface Signal	I/O
			5	SWO	Serial Wire Debug	Output
			6	CT69	Timer/counter 69	Output
			7	NCE69	IOMSTR N Chip Select 69	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
J2	F11	70	0	MSPI0_11	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE0	Serial Wire Debug Trace Output 0	Output
			2	-	-	-
			3	GPIO70	General purpose I/O	I/O
			4	MSPI2_1	MSPI Manager 2 Interface Signal	I/O
			5	COEX_GRANT	Coexistence Grant	Input
			6	CT70	Timer/counter 70	Output
			7	NCE70	IOMSTR N Chip Select 70	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
J1	F10	71	0	MSPI0_12	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE1	Serial Wire Debug Trace Output 1	Output
			2	-	-	-
			3	GPIO71	General purpose I/O	I/O
			4	MSPI2_2	MSPI Manager 2 Interface Signal	I/O
			5	COEX_REQ	Coexistence Request	Input
			6	CT71	Timer/counter 71	Output
			7	NCE71	IOMSTR N Chip Select 71	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K3	G11	72	0	MSPI0_13	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE2	Serial Wire Debug Trace Output 2	Output
			2	-	-	-
			3	GPIO72	General purpose I/O	I/O
			4	MSPI2_3	MSPI Manager 2 Interface Signal	I/O
			5	COEX_PRIORITY	Coexistence Priority Control	Input
			6	CT72	Timer/counter 72	Output
			7	NCE72	IOMSTR N Chip Select 72	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
K2	G10	73	0	MSPI0_14	MSPI Manager 0 Interface Signal	I/O
			1	SWTRACE3	Serial Wire Debug Trace Output 3	Output
			2	-	-	-
			3	GPIO73	General purpose I/O	I/O
			4	MSPI2_4	MSPI Manager 2 Interface Signal	I/O
			5	COEX_FREQ	Coexistence Frequency Control	Input
			6	CT73	Timer/counter 73	Output
			7	NCE73	IOMSTR/MSPI N Chip Select 73	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
K1	G9	74	0	MSPI0_15	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO74	General purpose I/O	I/O
			4	MSPI2_5	MSPI Manager 2 Interface Signal	I/O
			5	-	-	-
			6	CT74	Timer/counter 74	Output
			7	NCE74	IOMSTR N Chip Select 74	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
L3	H8	75	0	MSPI0_16	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO75	General purpose I/O	I/O
			4	MSPI2_6	MSPI Manager 2 Interface Signal	I/O
			5	-	-	-
			6	CT75	Timer/counter 75	Output
			7	NCE75	IOMSTR N Chip Select 75	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
L2	H9	76	0	MSPI0_17	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO76	General purpose I/O	I/O
			4	MSPI2_7	MSPI Manager 2 Interface Signal	I/O
			5	-	-	-
			6	CT76	Timer/counter 76	Output
			7	NCE76	IOMSTR N Chip Select 76	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
L1	H10	77	0	MSPI0_18	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO77	General purpose I/O	I/O
			4	MSPI2_9	MSPI Manager 2 Interface Signal	I/O
			5	-	-	-
			6	CT77	Timer/counter 77	Output
			7	NCE77	IOMSTR N Chip Select 77	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
F5	NC	78	0	MNCE0_0	MSPI Manager 0 nCE 0 Signal	-
			1	-	-	-
			2	-	-	-
			3	GPIO78	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT78	Timer/counter 78	Output
			7	NCE78	IOMSTR N Chip Select 78	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
H5	F6	79	0	MNCE0_1	MSPI Manager 0 nCE 1 Signal	-
			1	DISP_TE	Display TE input	Input
			2	ST_WCI_2W_TXD	BTDM	Output
			3	GPIO79	General purpose I/O	I/O
			4	ST_WCI_1W_RXD	BTDM	Output
			5	-	-	-
			6	CT79	Timer/counter 79	Output
			7	NCE79	IOMSTR N Chip Select 79	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	BTDM_TXEN	BTDM TX Enable	Output
			13	-	-	-
E5	NC	80	0	MNCE2_1	MSPI Manager 2 nCE 1 Signal	-
			1	DISP_TE	Display TE input	Input
			2	ST_WCI_2W_TXD	BTDM	Output
			3	GPIO80	General purpose I/O	I/O
			4	ST_WCI_1W_RXD	BTDM	Output
			5	-	-	-
			6	CT80	Timer/counter 80	Output
			7	NCE80	IOMSTR N Chip Select 80	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G3	D11	81	0	MSPI0_9	MSPI Manager 0 Interface Signal	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO81	General purpose I/O	I/O
			4	-	-	-
			5	-	-	-
			6	CT81	Timer/counter 81	Output
			7	NCE81	IOMSTR N Chip Select 81	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
N5	NC	82	0	SDIF0_CLKOUT	SD/SDIO/MMC Clock to Card (CLK)	Output
			1	-	-	-
			2	-	-	-
			3	GPIO82	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT82	Timer/counter 82	Output
			7	NCE82	IOMSTR N Chip Select 82	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
N2	NC	83	0	SDIF0_DAT0	SD/SDIO/MMC Data0 pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO83	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT83	Timer/counter 83	Output
			7	NCE83	IOMSTR/MSPI N Chip Select 83	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
N4	NC	84	0	SDIF0_DAT1	SD/SDIO/MMC Data1 pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO84	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT84	Timer/counter 84	Output
			7	NCE84	IOMSTR/MSPI N Chip Select 84	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
M2	NC	85	0	SDIF0_DAT2	SD/SDIO/MMC Data2 pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO85	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT85	Timer/counter 85	Output
			7	NCE85	IOMSTR/MSPI N Chip Select 85	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
N1	NC	86	0	SDIF0_DAT3	SD/SDIO/MMC Data3 pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO86	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT86	Timer/counter 86	Output
			7	NCE86	IOMSTR/MSPI N Chip Select 86	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
M5	NC	87	0	SDIF0_CMD	SD1/SD4/MMC Command pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO87	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT87	Timer/counter 87	Output
			7	NCE87	IOMSTR N Chip Select 87	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
H8	NC	88	0	DISP_ENB	Display enable signal for pixel memory (JDI)	Output
			1	-	-	-
			2	32KHzXT	32kHZ from analog	Output
			3	GPIO88	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	COEX_GRANT	Coexistence Grant	Input
			6	CT88	Timer/counter 88	Output
			7	NCE88	IOMSTR N Chip Select 88	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	DBIB_CSX	Display DBIB Chip Select	Output
G8	NC	89	0	DISP_XRST	Display Reset signal for Horizontal and Vertical drivers (JDI)	Output
			1	-	-	-
			2	-	-	-
			3	GPIO89	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	COEX_REQ	Coexistence Request	Input
			6	CT89	Timer/counter 89	Output
			7	NCE89	IOMSTR/MSPI N Chip Select 89	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	DBIB_DCX	Display DBIB Data/Command Selection	Output

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
J7	NC	90	0	DISP_R1	Display RGB Red Signal for even Pixels	Output
			1	-	-	-
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO90	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	COEX_PRIORITY	Coexistence Priority Control	Input
			6	CT90	Timer/counter 89	Output
			7	NCE90	-	-
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	DBIB_WRX	Display DBIB Write Enable	Output
K7	NC	91	0	DISP_R2	Display Even red data (JDI)	Output
			1	-	-	-
			2	CLKOUT	Oscillator output clock	Output
			3	GPIO91	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	COEX_FREQ	Coexistence Frequency Control	Input
			6	CT91	Timer/counter 89	Output
			7	NCE91	IOMSTR/MSPI N Chip Select 91	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	DBIB_RDX	Display DBIB Read Enable	Output
M9	NC	92	0	DISP_G1	Display RGB Green Signal for even Pixels	Output
			1	-	-	-
			2	DISP_QSPI_D0	Display SPI Data0	Bidirectional
			3	GPIO92	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	DISP_SPI_SD	Display SPI Data Out	Bidirectional
			6	CT92	Timer/counter 89	Output
			7	NCE92	IOMSTR N Chip Select 92	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	DISP_SPI_SDO	Display SPI Data Out	Output
			13	DISP_QSPI_D0_OUT	Display SPI Data0	Output

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
M8	NC	93	0	DISP_G2	Display Even green data (JDI)	Output
			1	-	-	-
			2	DISP_QSPI_D1	Display SPI Data1	Output
			3	GPIO93	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	DISP_SPI_DCX	Display SPI DCx	Output
			6	CT93	Timer/counter 89	Output
			7	NCE93	IOMSTR/MSPI N Chip Select 93	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	DBIB_D0	Display DBIB Data 0	Output
J8	NC	94	0	DISP_B1	Display RGB Blue Signal for even Pixels	Output
			1	-	-	-
			2	DISP_QSPI_SCK	Display SPI CLK	Output
			3	GPIO94	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	DISP_SPI_SCK	Display SPI Clock	Output
			6	CT94	Timer/counter 89	Output
			7	NCE94	IOMSTR N Chip Select 94	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	DBIB_D1	Display DBIB Data 1	Output
L10	NC	95	0	DISP_B2	Display Even blue data (JDI)	Output
			1	-	-	-
			2	DISP_QSPI_D2	Display SPI Data2	Output
			3	GPIO95	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	DISP_SPI_SDI	Display SPI Data IN	input
			6	CT95	Timer/counter 89	Output
			7	NCE95	IOMSTR N Chip Select 95	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	RF_XCVR_TST1	BTDM DSP Diagnostic Test	Output
			13	DBIB_D2	Display DBIB Data 2	Output

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
L9	NC	96	0	DISP_HST	Display Horizontal Start signal (JDI)	Output
			1	-	-	-
			2	DISP_QSPI_D3	Display SPI Data3	Output
			3	GPIO96	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	DISP_SPI_RST	Display SPI Reset	Output
			6	CT96	Timer/counter 89	Output
			7	NCE96	IOMSTR N Chip Select 96	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	RF_XCVR_TST2	BTDM DSP Diagnostic Test	Output
			13	DBIB_D3	Display DBIB Data 3	Output
L7	NC	97	0	DISP_VST	Display Veritical Start signal (JDI)	Output
			1	-	-	-
			2	-	-	-
			3	GPIO97	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT97	Timer/counter 89	Output
			7	NCE97	IOMSTR N Chip Select 97	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	RF_XCVR_TST3	BTDM DSP Diagnostic Test	Output
			13	DBIB_D4	Display DBIB Data 4	Output
K11	NC	98	0	DISP_HCK	Display Horizontal Shift clock (JDI)	Output
			1	-	-	-
			2	-	-	-
			3	GPIO98	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT98	Timer/counter 89	Output
			7	NCE98	IOMSTR N Chip Select 98	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	DBIB_D5	Display DBIB Data 5	Output

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
K10	NC	99	0	DISP_VCK	Display Vertical Shift clock (JDI)	Output
			1	-	-	-
			2	ST_WCI_2W_RXD	BTDM DSP Diagnostic Test	Output
			3	GPIO99	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT99	Timer/counter 89	Output
			7	NCE99	IOMSTR N Chip Select 99	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	BTDM_TXEN	BTDM TX Enable	Output
			13	DBIB_D6	Display DBIB Data 6	Output
K8	NC	100	0	DISP_TE	Display TE input	Input
			1	ST_WCI_1W_RXD	BTDM	Output
			2	ST_WCI_2W_TXD	BTDM	Output
			3	GPIO100	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT100	Timer/counter 100	Output
			7	NCE100	IOMSTR N Chip Select 100	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	BTDM_RXEN	BTDM RX Enable	Output
			13	DBIB_D7	Display DBIB Data 7	Output
L8	NC	101	0	DISP_QSPI_CS_N	Display QSPI Chip Select	Output
			1	-	-	-
			2	BTDM_TXEN	BTDM TX Enable	Output
			3	GPIO101	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	DISP_SPI_CS_N	Display SPI Chip Select	Output
			6	CT101	Timer/counter 101	Output
			7	NCE101	IOMSTR N Chip Select 101	Output
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	ST_WCI_1W_RXD	BTDM	Output
			13	ST_WCI_2W_TXD	BTDM	Output

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
G10	NC	102	0	SLFDSCK	SPI Slave Full Duplex clock	Input
			1	SLFDSCL	I2C Slave Full Duplex clock	Input
			2	PDMI2S0_CLK	PDMI2S0 Bit clock	Bidirectional
			3	GPIO102	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT102	Timer/counter 102	Output
			7	NCE102	IOMSTR N Chip Select 102	Output
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	DBIB_D8	Display DBIB Data 8	Output
F10	NC	103	0	SLFDMOSI	SPI Slave Full Duplex input data	Input
			1	SLFDSDAWIR3	I2C Slave Full Duplex I/O data (I2C) 3 Wire Data (SPI)	Bidirectional Open Drain
			2	PDMI2S0_SDOUT	PDMI2S0 Data output	Output
			3	GPIO103	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT103	Timer/counter 103	Output
			7	NCE103	IOMSTR N Chip Select 103	Output
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	DBIB_D9	Display DBIB Data 9	Output
F11	NC	104	0	SLFDMISO	SPI Slave Full Duplex output data	Output
			1	BTDM_TXEN	BTDM TX Enable	Output
			2	PDMI2S0_WS	PDMI2S0 L/R clock	Bidirectional
			3	GPIO104	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT104	Timer/counter 104	Output
			7	NCE104	IOMSTR N Chip Select 104	Output
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	DBIB_D10	Display DBIB Data 10	Output

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
C9	NC	105	0	SLFDnCE	SPI Slave Full Duplex chip enable	Input
			1	BTDM_RXEN	BTDM RX Enable	Output
			2	-	-	-
			3	GPIO105	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT105	Timer/counter 105	Output
			7	NCE105	-	-
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	DBIB_D11	Display DBIB Data 11	Output
H10	NC	106	0	SLFDINT	Configurable Slave Interrupt	Output
			1	I2S0_MCLK	I2S0 MCLK`	Bidirectional
			2	-	-	-
			3	GPIO106	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	ST_WCI_2W_RXD	BTDM DSP Diagnostic Test	Output
			6	CT106	Timer/counter 106	Output
			7	NCE106	-	-
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	DBIB_D12	Display DBIB Data 12	Output
F12	B4	107	0	PDM0_CLK	PDM0 Clock output	Output
			1	-	-	-
			2	-	-	-
			3	GPIO107	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT107	Timer/counter 107	Output
			7	NCE107	-	-
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	DBIB_D13	Display DBIB Data 13	Output

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
E12	A4	108	0	PDM0_DATA	PDM0 audio data input to chip	Input
			1	-	-	-
			2	-	-	-
			3	GPIO108	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT108	Timer/counter 108	Output
			7	NCE108	-	-
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	DBIB_D14	Display DBIB Data 14	Output
G12	NC	109	0	I2S0_CLK	I2S0 Bit clock	Bidirectional
			1	PDMI2S0_CLK	PDMI2S0 Bit clock	Bidirectional
			2	-	-	-
			3	GPIO109	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	-	-	-
			6	CT109	Timer/counter 109	Output
			7	NCE109	-	-
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	DBIB_D15	Display DBIB Data 15	Output
G5	E7	110	0	MNCE2_0	MSPI Manager 2 nCE 0 Signal	-
			1	-	-	-
			2	-	-	-
			3	GPIO110	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT110	Timer/counter 110	Output
			7	NCE110	-	-
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
H4	NC	111	0	MNCE2_1	MSPI Manager 2 nCE 1 Signal	-
			1	-	-	-
			2	-	-	-
			3	GPIO111	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	ST_WCI_2W_RXD	BTDM DSP Diagnostic Test	Output
			6	CT111	Timer/counter 111	Output
			7	NCE111	-	-
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	BTDM_RXEN	BTDM RX Enable	Output
			13	-	-	-
M1	NC	112	0	MSPI2_8	MSPI Manager 2 Interface Signal	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO112	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	-	-	-
			6	CT112	Timer/counter 112	Output
			7	NCE112	-	-
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-
E6	NC	113	0	DISP_QSPI_CS_N	Display QSPI Chip Select	Output
			1	-	-	-
			2	ST_WCI_2W_RXD	BTDM DSP Diagnostic Test	Output
			3	GPIO113	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	DISP_SPI_CS_N	Display SPI Chip Select	Output
			6	CT113	Timer/counter 113	Output
			7	NCE113	-	-
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	BTDM_TXEN	BTDM TX Enable	Output
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
N3	NC	114	0	SDIF0_DAT4	SD/SDIO/MMC Data4 pin	I/O
			1	-	-	-
			2	BTDM_TXEN	BTDM TX Enable	Output
			3	GPIO114	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	-	-	-
			6	CT114	Timer/counter 114	Output
			7	NCE114	-	-
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	-	-	-
			13	-	-	-
M3	NC	115	0	SDIF0_DAT5	SD/SDIO/MMC Data5 pin	I/O
			1	-	-	-
			2	BTDM_RXEN	BTDM RX Enable	Output
			3	GPIO115	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	-	-	-
			6	CT115	Timer/counter 115	Output
			7	NCE115	-	-
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
M4	NC	116	0	SDIF0_DAT6	SD/SDIO/MMC Data6 pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO116	General purpose I/O	I/O
			4	TRIG2	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT116	Timer/counter 116	Output
			7	NCE116	-	-
			9	UART0_TX	UART0 transmit output	Output
			10	UART1_CTS	UART1 Clear to Send (CTS) input	Input
			12	-	-	-
			13	-	-	-

Table 24: Apollo510 Lite Series SoCs Pin List and Function Table

BGA PIN	CSP Pin	GPIO Pad No.	Fcn Select No.	Pad Function Name	Description	Pin Type
M6	NC	117	0	SDIF0_DAT7	SD/SDIO/MMC Data7 pin	I/O
			1	-	-	-
			2	-	-	-
			3	GPIO117	General purpose I/O	I/O
			4	TRIG3	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT117	Timer/counter 117	Output
			7	NCE117	-	-
			9	UART0_RX	UART0 receive input	Input
			10	UART1_RTS	UART1 Request to Send (RTS)	Output
			12	-	-	-
			13	-	-	-
H9	NC	118	0	I2S0_MCLK	I2S0 MCLK`	Bidirectional
			1	-	-	-
			2	PDMI2S0_CLK	PDMI2S0 Bit clock	Bidirectional
			3	GPIO118	General purpose I/O	I/O
			4	TRIG0	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT118	Timer/counter 118	Output
			7	NCE118	-	-
			9	UART1_TX	UART1 transmit output	Output
			10	UART0_CTS	UART0 Clear to Send (CTS)	Input
			12	I2S0_CLK	I2S0 Bit clock	Bidirectional
			13	-	-	-
F7	NC	119	0	-	-	-
			1	-	-	-
			2	BTDM_RXEN	BTDM RX Enable	Output
			3	GPIO119	General purpose I/O	I/O
			4	TRIG1	ADC trigger input	Input
			5	SWO	Serial Wire Debug	Output
			6	CT119	Timer/counter 119	Output
			7	NCE119	-	-
			9	UART1_RX	UART1 receive input	Input
			10	UART0_RTS	UART0 Request to Send (RTS)	Output
			12	ST_WCI_2W_RXD	BTDM DSP Diagnostic Test	Output
			13	-	-	-

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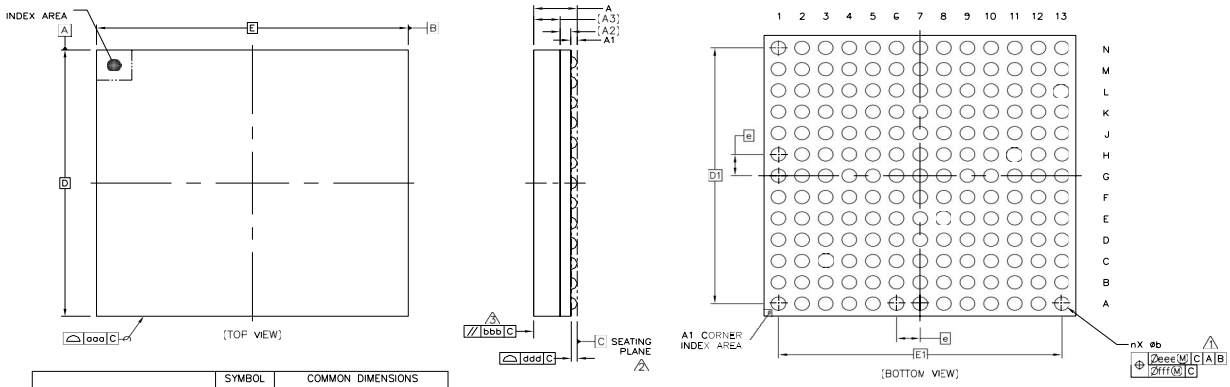
29. Package Mechanical Information[1]

29.1 Apollo510 Lite Series SoCs BGA Package



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.676	0.74	0.8
STAND OFF	A1	0.07	---	0.15
SUBSTRATE THICKNESS	A2		0.18	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		5.3	BSC
	E		5.3	BSC
BALL DIAMETER			0.2	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.4	BSC
BALL COUNT	n		169	
EDGE BALL CENTER TO CENTER	D1		4.8	BSC
	E1		4.8	BSC
BODY CENTER TO CONTACT BA	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.1	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.05	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 57. BGA Package Drawing for Apollo510 Lite Series SoCs

1. All dimensions in mm unless otherwise noted.

29.1.1 Apollo510 Lite Series SoCs BGA Package Top Side Marking

Package type: 5.3 mm x 5.3 mm (0.8 mm max thickness), 169-pin BGA

Part Number: AP510NLA-CBR, AP510BLA-CBR or AP510DLA-CBR

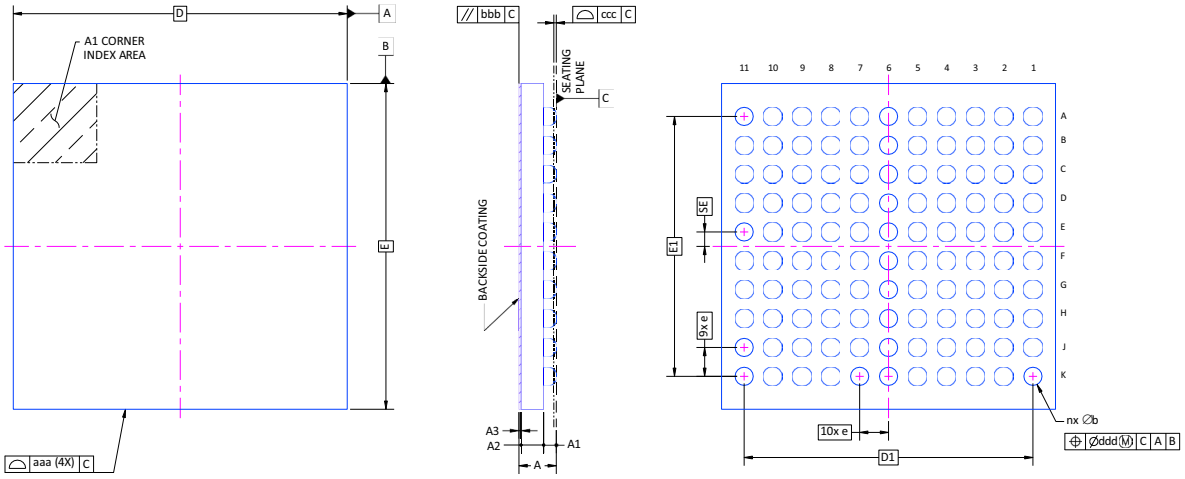
Memory Size: 2 MB

Figure 58. Apollo510 Lite Series SoCs BGA Package Top Side Marking

Table 25: Apollo510 Lite Series SoCs BGA Marking Description

Line	Field	Description
1	Part Description	Memory Size: 2M
2	Part Name	AP510NLA, AP510BLA or AP510DLA
3	YY = Year WW = Work Week XX = Sequential Lot Number	YY corresponds to the year. WW is the release week of assembly lot. XX is the sequential lot number assigned by the assembly house
4	R = Production Revision F = Foundry Site A = Assembly Site T = Test Site	RFAT designates the product revision and the supply chain.

29.2 Apollo510 Lite Series SoCs WLCSP Package



TOP VIEW SIDE VIEW BOTTOM VIEW

Control Dimensions are in Millimeter

		Symbol	Common Dimensions		
			MIN.	NOM.	MAX
Total Thickness		A	0.394	0.452	0.510
Stand Off		A1	0.122	---	0.182
Wafer Thickness		A2	0.250	0.275	0.300
Film Thickness		A3	0.022	0.025	0.028
Body Size	X	D	4.047		
	Y	E	3.948		
Ball / Bump Pitch	X	SD	---		BSC
	Y	SE	0.175		BSC
Edge Ball Center to Center	X	D1	3.50		BSC
	Y	E1	3.15		BSC
Pitch		e	0.350		BSC
Ball Diameter (Size)			0.20		
Ball / Bump Width		b	0.197	---	0.250
Ball / Bump Count		n	110		
Package Edge Tolerance		aaa	0.03		
Wafer Flatness		bbb	0.06		
Coplanarity		ccc	0.03		
Ball / Bump Offset (Package)		ddd	0.015		

NOTE :

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL PRIMARY DATUM C.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
3. THIS POD IS WITH BACKSIDE COATING

Figure 59. WLCSP Package Drawing for Apollo510 Lite Series SoCs

29.2.1 Apollo510 Lite Series SoCs WLCSP Package Top Side Marking

Package type: 4.047 mm x 3.948 mm (0.510 mm max thickness), 110-pin WLCSP

Part Number: AP510NLA-CCR, AP510BLA-CCR or AP510DLA-CCR

Memory Size: 2 MB

Figure 60. Apollo510 Lite Series SoCs WLCSP Package Top Side Marking

Table 26: Apollo510 Lite Series SoCs WLCSP Marking Description

Line	Field	Description
1	Part Description	Memory Size: 2M
2	Part Name	AP510NLA, AP510BLA or AP510DLA
3	YY = Year WW = Work Week XX = Sequential Lot Number	YY corresponds to the year. WW is the release week of assembly lot. XX is the sequential lot number assigned by the assembly house
4	R = Production Revision F = Foundry Site A = Assembly Site T = Test Site	RFAT designates the product revision and the supply chain.

29.3 Reflow Profile

Table 27 lists the reflow conditions for the lead-free package. Reference IR Reflow Profile for Moisture Sensitivity Test (J-STD-020).

Reflow times: 3 cycles

Table 27: Reflow Condition (260 °C) for Pb-free Package

Profile Features	Pb-Free Assembly
Average ramp-up rate (include 217°C to Peak)	3°C/second max.
Temperature maintained above 217°C	60 to 150 seconds
Time within 5°C of actual peak temperature	20 - 40 seconds
Peak temperature (minimum)	260 +0/-5°C
Ramp-down rate	6°C /second max.
Time 25°C to peak temperature	8 minutes max.

Figure 61 illustrates the temperature profile for reflow soldering requirements.

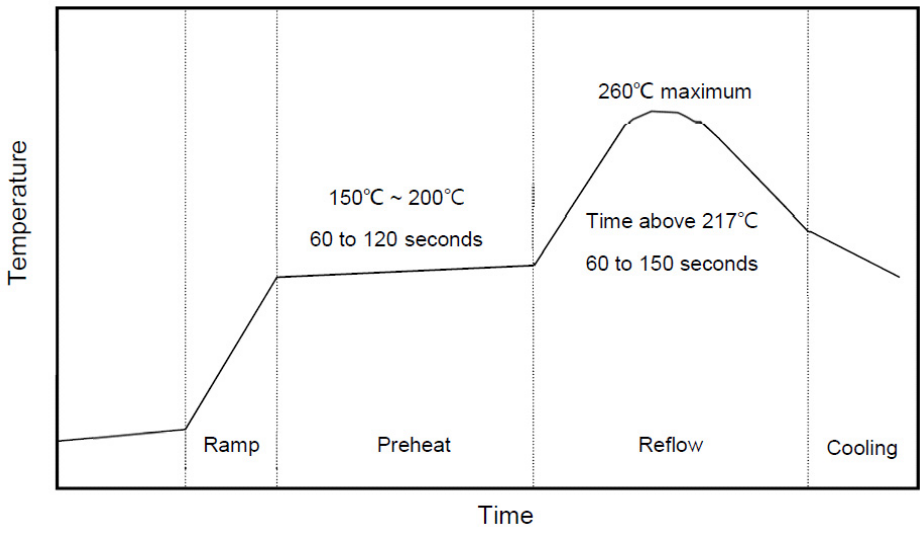


Figure 61. Reflow Profile

30. Electrical Characteristics

IMPORTANT NOTICE

Specifications and other information in this Apollo510 Lite Series Datasheet are preliminary and subject to change.

Contact Ambiq sales with questions about specifications.

30.1 Absolute Maximum Ratings

The absolute maximum ratings are the limits to which the device can be subjected without permanently damaging the device and are stress ratings only. Device reliability may be adversely affected by exposure to absolute-maximum ratings for extended periods. Functional operation of the device at the absolute maximum ratings or any other conditions beyond the recommended operating conditions is not implied.

Table 28: Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
VDDP	SIMO/LDO Buck Supply voltage		-0.2	3.63	V
VDDA	Analog Supply voltage				
VDDH	High voltage domain supply voltage				
VDDH1	High voltage domain 1 IO Supply voltage		-0.2	3.63	V
VDDH2	High voltage domain 2 IO Supply voltage		-0.2	3.63	V
VDDH3	High voltage domain 3 IO Supply voltage		-0.2	3.63	V
VDDH4	High voltage domain 4 IO Supply voltage		-0.2	3.63	V
VDDH5	High voltage domain 5 IO Supply voltage		-0.2	3.63	V
VDD18	MIPI, DSI, DISPPLL Supply voltage		-0.2	1.98	V
VDDRF_TRX	RF Core Supply (sourced from SIMO Buck VDDRF output)		-0.2	1.98	V
VDDRF_PAH	RF High-Power PA Supply voltage (sourced from external regulator)		-0.2	1.98	V
VDDUSB33	USB Analog 3.3 V Supply voltage		-0.2	3.63	V
VDDUSB0P9	USB Analog 0.9 V Supply voltage		-0.2	0.99	V
V_{IO}	Voltage on all input and output pins		-0.30	VDDHn[1] + 0.30	V
$VDDX_{FSLEW}$	Falling slew rate for VDDP, VDDA, VDDH and VDDHn power supplies		-	2	kV/s
T_{OPEC}	Extended commercial operating temperature range	Specific to extended commercial temperature range SKUs	-20	70	ºC
T_{OPI}	Industrial operating temperature range	Specific to industrial temperature range SKUs	-40	85	ºC
T_{REFLOW}	Reflow temperature	Reflow Profile per JEDEC J-STD-020D.1	-	260	ºC
I_{LU}	Latch-up current	EIA/JESD78, 25°C, ±100 mA trigger current and Over voltage at 1.5 Vmax	-	100	mA
V_{ESDHBM}	ESD Human Body Model (HBM)	JS-001-2017	-	2000	V
V_{ESDCDM}	ESD Charged Device Model (CDM)	JS-002-2014	-	250	V

1. The designation “n” corresponds to the voltage source for the pin, e.g., VDDH1. This specification is for all VDDH supplies powering GPIO.

30.2 Recommended Operating Conditions

30.2.1 External Voltage Supplies

Table 29: External Voltage Supplies

Supply	Description	Source	Min	Typ	Max	Units	Notes
VDDA	Analog Supply	Battery / External Regulator	1.71	1.8	2.20	V	VDDA, VDDP and VDDH must be connected to the same supply.
VDDP	SIMO/LDO Buck Supply						
VDDH	High voltage domain supply voltage						
VDDH1	Secondary I/O Supply (Primary Interface: HWTRACE)	Battery / External Regulator	1.71	1.8	2.20	V	Must be tied to VDDH if not in use.
VDDH2	Secondary I/O Supply; supplies I3C	Battery / External Regulator	1.71	1.8	2.20	V	VDDH2 must be at the same voltage as VDDH. Must be tied to VDDH if not in use.
VDDH3	Secondary I/O Supply (Primary Interface: MSPI0)	Battery / External Regulator	1.14	1.2 / 1.8	2.20	V	Must be no lower than 1.71 V when powering an MSPI instance. Must be tied to VDDH if not in use.
VDDH4	Secondary I/O Supply	Battery / External Regulator	1.71	1.8 / 3	3.63	V	Must be tied to VDDH if not in use.
VDDH5	Secondary I/O Supply (Primary Interface: MiP Display)	Battery / External Regulator	1.71	1.8 / 3	3.63	V	Must be tied to VDDH if not in use.
VDD18	MIPI DPHY LP LDO and transceivers	Battery / External Regulator	1.62	1.8	1.98	V	Noise/ripple: ± 2% (72mVpk-pk) Frequency range: 10 MHz - 3 GHz Leakage current: 2-3 µA (typ)[1]
VDDRF_H	RF High Voltage Supply	External Regulator	1.71	1.8	1.98	V	
VDDRF_TRX	RF Core Supply	VDDRF rail of SIMO Buck	0.95	1.05	1.25	V	
VDDRF_PAH	RF High-Power PA Supply	External Regulator	1.65	1.8	1.98	V	For non-radio SKUs this rail should be tied to ground.
VDDUSB33	USB Analog 3.3 V Supply	Battery / External Regulator	3.0	3.3	3.63	V	See following section 30.2.1.1
VDDUSB0P9	USB Analog 0.9 V Supply	Internal LDO	0.84	0.9	0.99	V	Noise/ripple: < 3% (pk-pk). See following section 30.2.1.1

1. A load switch could be used for this rail to decrease current if the stated leakage current is too high for the targeted use case. It is recommended to use a low-leakage external switch controlled by the MCU, such as:.
   - TI TPS22916xx, I_q = 10 nA typ
   - Toshiba TCK106AG/107AG/108AG, I_q = 14 nA typ.
   - Microchip MIC94080/1/4/5, I_q = 20 nA typ.

30.2.1.1 USB Supplies

The following points should be considered when configuring USB power or when not using the USB. Connection and termination requirements and options are different on the BGA and WLCSP packages and are addressed separately below.

BGA Package:

Figure 62 depicts the USB power configuration options for the BGA.

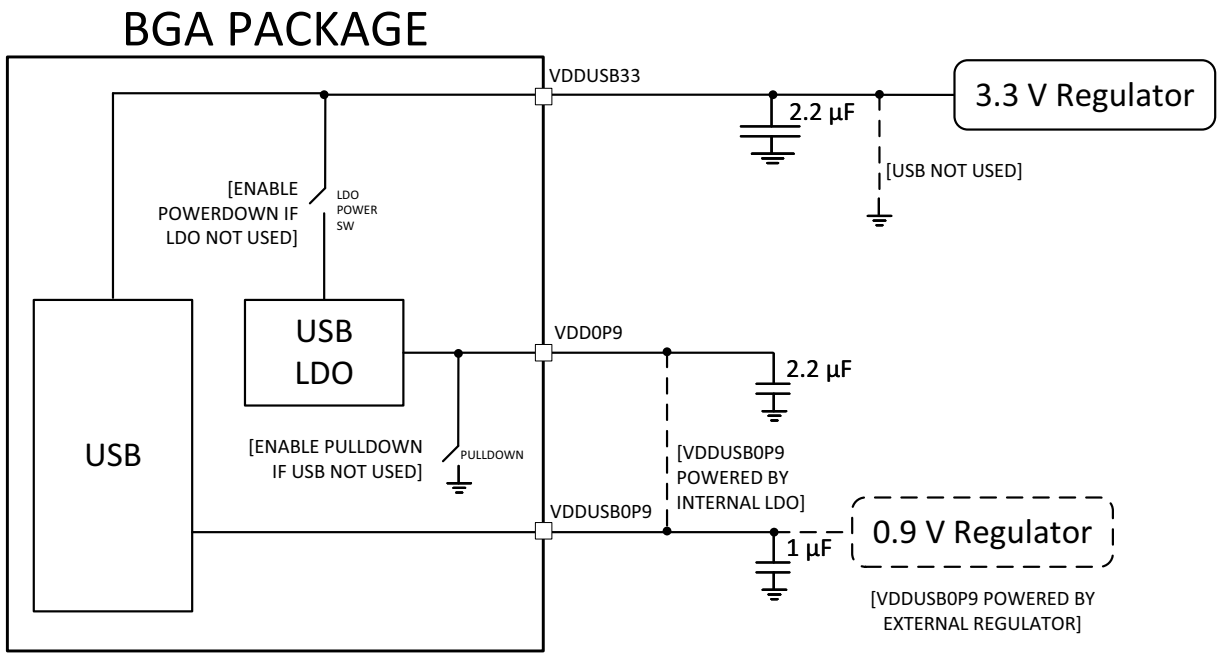


Figure 62. USB Power Options on the BGA Package

- VDDUSB33 is the USB's 3.3 V supply and also is the input to an internal LDO which sources the VDD0P9 output pin. This VDD0P9 output pin can be selected as the USB's 0.9 V supply and connected to the VDDUSB0P9 input pin.
- VDDUSB33 should have a 2.2 µF decoupling capacitor if USB is to be used.
- VDD0P9 is pinned out only on the BGA package and should have a 2.2 µF bypass capacitor if the USB's internal LDO is to be used.
- VDDUSB0P9 can be connected to the VDD0P9 output. Alternatively, though not preferred, VDDUSB0P9 can be sourced externally and not connected to VDD0P9, and the USB LDO should be put in its power-down state (MCUCTRL_USBLDOCTRL_USBLDOPDNB = EN).
- VDDUSB0P9 may require a bypass capacitor so pads/connections should be included on the PCB if filtering is needed. The bypass capacitor is not needed and should not be used if VDDUSB33 is grounded (USB not used). See next two bullets.
- When VDDUSB33 is disabled/powered off by the system PMIC and when VDDUSB0P9 is connected to VDD0P9, VDDUSB0P9 should be pulled down to ground through the internal software-controlled discharge resistor. If not connected to VDD0P9, VDDUSB0P9 should be pulled to ground through a load-switch or PMIC discharge resistor.
- VDDUSB0P9 and VDDUSB33 should be pulled down to ground when the USB is not in use. If VDD0P9 is connected to VDDUSB0P9, the internal VDD0P9 pull-down resistor (MCUCTRL_USBLDOCTRL_USBLDOPULLDNDIS = EN) may be used for this purpose.

- The LDO output (VDD0P9 pin on the BGA) should never be tied to ground if VDDUSB33 is powered. VDD0P9 functionality allows disabling the LDO output and terminating it through a pull-down resistor.

WLCSP Package:

Figure 63 depicts the USB power configuration options for the WLCSP.

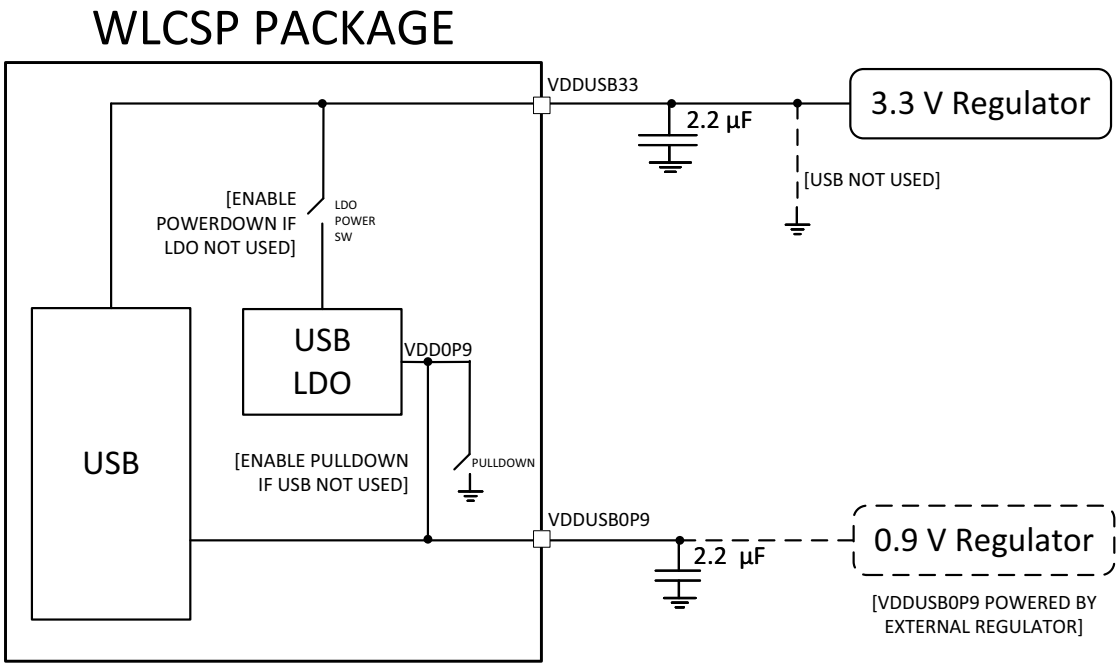


Figure 63. USB Power Options on the WLCSP Package

- VDDUSB33 is the USB's 3.3 V supply and also is the input to an internal LDO which sources the 0.9 V VDD0P9 internally.
- VDDUSB33 should have a 2.2 µF decoupling capacitor if USB is to be used.
- VDD0P9 is sourced from the internal LDO to provide 0.9 V for VDDUSB0P9. It is not pinned out on the WLCSP package.
- VDDUSB0P9 is connected internally to the VDD0P9 output. If VDDUSB0P9 is to be sourced externally (not needed or recommended), the USB LDO should be put in its power-down state (MCUCTRL_USBLDOCTRL_USBLDOPDNB = EN).
- When VDDUSB33 is disabled/powered off by the system PMIC, and since VDDUSB0P9 is tied to VDD0P9, VDDUSB0P9 should be programmatically pulled down to ground through the internal software-controlled pull-down resistor (MCUCTRL_USBLDOCTRL_USBLDOPULLDNDIS = EN).
- VDDUSB0P9 should have a 2.2 µF bypass capacitor if USB is to be used. It is not needed and should not be used if VDDUSB33 is grounded (USB not used). See next two bullets.
- VDDUSB33 should be pulled down to ground when the USB is not in use, and VDDUSB0P9 should be left open. VDD0P9 is internally connected to VDDUSB0P9, so the internal VDD0P9 pull-down resistor may be used to pull the input down.
- The LDO output (VDDUSB0P9 pin on the WLCSP) should never be tied to ground if VDDUSB33 is powered. VDD0P9 functionality allows disabling the LDO output and terminating it through the pull-down resistor.

30.2.2 Recommended External Components for Voltage Supplies

30.2.2.1 Components for External Voltage Supplies

Table 30: Recommended Bypass Capacitors for External Supplies

External Supply	Bypass Capacitor
VDDH, VDDH1, VDDH2, VDDH5	2.2 µF to ground
VDDH3	4.7 µF to ground
VDDH4	4.7 µF to ground
VDDA	1 µF to ground
VDDP	10 µF to ground (SIMO Buck converter input capacitance - C_{PB})
VDDUSB33	2.2 µF to ground
VDDUSB0P9	2.2 µF to ground
VDD18	2.2 µF to ground
VDDRF_H	4.7 µF to ground, plus 10 nF high frequency filtering capacitor (see note)
VDDRF_PAH	10 µF to ground, plus 10 nF high frequency filtering capacitor (see note)
VDDRF_TRX	4.7 µF to ground, plus 10 nF high frequency filtering capacitor (see note)

Additional Notes:

1. For VDDH3 and VDDH4, it might be possible to use a bypass capacitor smaller than 4.7 µF (possibly 2.2 µF) depending on the speed of the external LDO and how close the LDO is placed to the Apollo510 device and external PSRAM power pins, and the interface speed being used. It is also recommended that the same size bypass capacitor be used for the I/O supply of the external (PSRAM) device.
2. For VDDP 10 µF: Recommend 0402 package, 10 V. No more than 40% reduction in capacitance (6.0 µF) with a DC bias of 1.8 V. Suitable component: CL05A106MP8NUB8.
3. Recommend use of 5 V or greater capacitors for 1.9 V rails
4. Recommend use of 10 V capacitors for 3.3 V rails
5. Do not float any supply input. If a supply is not used, it should be tied to a supply within its operating range.
6. With the preconditions that HP mode and GPU are not used, Tx power is limited to <= 4 dBm, and VDDC, VDDC_LV, VDDF, VDDS and VDDRF capacitors are 4.7 µF / 6.3 V / X5R / 0201 (e.g., https://www.digikey.com/en/products/detail/murata-electronics/GRM035R60J475ME15J/10699045?msockid=39be6f620b1868a53b727b560ab96914), then the following capacitor characteristics can be used:
   - VDDRF_H, VDDRF_PAH, and VDDRF_TRX high frequency filtering capacitors should be 10 nF / 6.3 V with size 0201.
   - VDDRF_H, VDDRF_PAH, and VDDRF_TRX bulk capacitors should be size 0201 with the following values:
     - VDDRF_TRX: 4.7 µF / 6.3 V
     - VDDRF_H: 4.7 µF / 6.3 V
     - VDDRF_PAH: 10 µF / 4 V
7. Suitable standalone small form factor LDOs:
   - Microchip MCP1811A in 1.0 x 1.0 x 0.50 mm UDFN package
   - TI TPS7A02 in 1.0 x 1.0 x 0.40 mm X2SON package

30.2.2.2 Components for SIMO Buck Converter

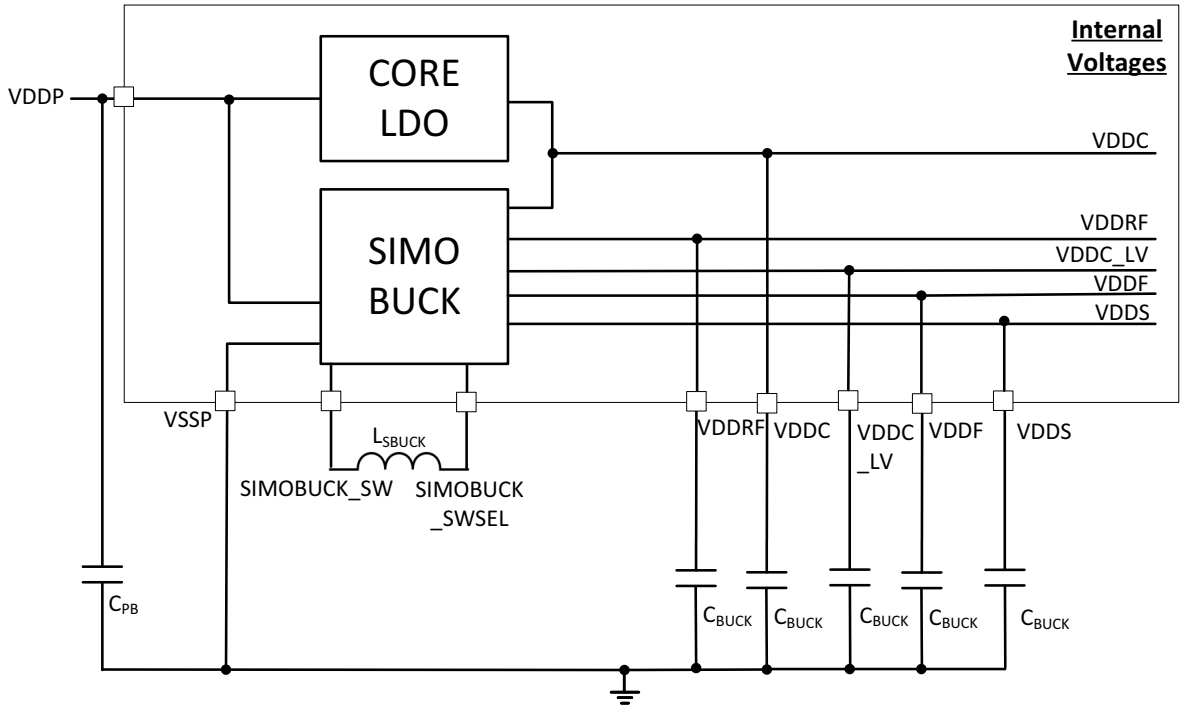


Figure 64. External Components for SIMO Buck

Table 31: SIMO Buck Converter External Components

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
L_{SBUCK}	SIMO Buck converter inductance (V_{SIMO})		-	2.2	-	µH
C_{BUCK}	SIMO Buck converter output capacitance (5) (VDDC, VDDC_LV, VDDF, VDDS, VDDRF)		-	4.7/10	-	µF

NOTES:

1) For operation across the full voltage and temperature range, the SIMO Buck Inductor (L_{SBUCK} connected between SIMOBUCK_SW and SIMOBUCK_SWSEL) with the following characteristics is required:

- 2.2 µH
- Saturation current >= 1 A
- Maximum DC resistance < 550 mΩ
- Operating frequency range > 20 MHz
- Recommended[1] parts:
  - Murata DFE201210U-2R2M=P2 (0805 size)
  - Taiyo Yuden LSCND1608HKT2R2MF (0603 size)
- Other options (all 2.2 µH):

Table 32: SIMO Buck Converter Inductor Options

Part Number	Manufacturer	DCR (mOhm)	Current Rating (Amps)	Saturation Current (Amps)	Footprint	L x W x H (in)
DFE201210U-2R2M=P2	Murata	228	1.2	2	0805	0.079 x 0.047 x 0.039
LSCND1608HKT2R2MF	Taiyo Yuden	250	1.4	1.3	0603	0.063 x 0.031 x 0.031
DFE252012F-2R2M=P2	Murata	82	2.3	3.3	1008	0.098 x 0.079 x 0.047
74479276222C	Wurth Elektronik	135	1.6	2.5	0806	0.079 x 0.063 x 0.039
CIGT201610EH2R2MNE	Samsung	87	2.5	2.9	0806	0.079 x 0.063 x 0.039
DFE21CCN2R2MELL	Murata	138	1.8	2.1	0805	0.079 x 0.047 x 0.031
AOTA-B201610S2R2MT	Abracon	74	2.0	2.6	0806	0.079 x 0.063 x 0.039

2) For C_{PB} and C_{BUCK} the following specifications should be followed

- Smaller package option: 4.7 µF, ±20%,6.3 V, X5R, -55°C ~ 85°C, ceramic
- 0201 package to be placed as close to the MCU pins as possible
- No more than 20% reduction in capacitance with a DC bias of 0.9 V
- Recommended parts:
  - Murata GRM035R60J475ME15 or equivalent

Larger package option for up to 2% reduction in total power over smaller package:

- 10 µF, ±20%, 10 V, X5R, -55°C ~ 85°C, ceramic
- 0402 package to be placed as close to the MCU pins as possible
- No more than 20% reduction in capacitance with a DC bias of 0.9 V
- Recommended parts:
  - Murata GRT155R61A106ME13J or equivalent

1. Inductors with higher Q rating (Q > 20 between 2 MHz and 10 MHz) are recommended. Inductors with lower Q may be used, but will result in power consumption increase of a few percent.

30.2.3 Power Sequencing

Table 33: Power Supply Sequencing

External Supply[1]	Conditions/Notes
VDDP/VDDH/VDDA[2]	1. Power up concurrently from same source to the same voltage (i.e., VDDP = VDDH = VDDA). 2. Should generally be supplied at nearly the same time as other rails. 3. Some skew is acceptable.
VDDH1-VDDH5[2]	1. May be powered up before, or at the same time as, VDDP/VDDH/VDDA are powered[3]. 2. May be a separate supply from VDDP/VDDH/VDDA, but it may be tied to VDDP/VDDH/VDDA if not requiring a different voltage.
VDD18	1. Should be tied to ground if not using MIPI DSI interface[4]. 2. If using MIPI, then may be powered at the same time as VDDP/VDDH/VDDA but not before. 3. Preferably only enabled/powered up when the display is being used.
VDDUSB33/ VDDUSB0P9	1. May be powered before, at the same time as, or after VDDP/VDDH/VDDA. 2. For USB power details, see USB chapter and USB PHY specifications later in this chapter. 3. Only required when using USB (i.e., when USB cable is plugged in). 4. Powering both supplies at the same time from VBUS source is recommended, with 0.9 V generated by LDO from the 3.3 V.[5]
VDDRF_H/ VDDRF_TRX/ VDDRF_PAH	1. Radio Subsystem power rails VDDRF_H and VDDRF_PAH (unless this rail is dynamically switched by RF direction signal for power saving) must be powered up before initiating the Cortex-M55 power-on sequence starting with powering on the VDDRF_TRX rail (enabling the SIMO Buck VDDRF output) by enabling the SIMO Buck via the system PWRCTRL_VRCTRL register.

1. Recommended termination of unused interface:
   - USB data pads (USB0PP and USB0PN) left open
   - Both USB PHY power rails VDDUSB33 and VDDUSB0P9 connected to ground
   - DSI TX data and clock pads left open
2. Falling slew rate for these supplies cannot exceed 2 kV/s.
3. Grounding any of these supplies while VDDP/VDDH/VDDA are powered will result in excess current draw and can have long term reliability implications. It is acceptable to have one VDDHn rail ramp up *after* VDDP/VDDH/VDDA as long as that rail ramps up while the CPU is still in reset (nRST pin is low).
4. Note that VDD18 leakage current is 2-3 µA (typ).
5. Although it is recommended to power-up VDDUSB33 and VDDUSB0P9 together only when USB is to be used, it is possible to keep VDDUSB33 powered at all times. In which case it is required that a 2 MΩ pull-down resistor be included on each of the USB data lines to prevent leakage current. Note that in all cases, to minimize leakage current, the USB internal power rail must be enabled by software before external power is applied to VDDUSB0P9.

30.3 Current Consumption

Table 34: Current Consumption in Active Mode and Sleep Modes

Symbol	Parameter	Test Conditions[1,2]	VDD (V)	Min	Typ	Max	Unit
$I_{RUNLPFB}$	Coremark run current in low power mode	Executed from internal MRAM, cache enabled, SIMO buck enabled, core clock/HFRC=96 MHz, 128 kB TCM enabled, radio subsystem off	1.8	-	34.5	-	µW/ MHz
$I_{RUNHPFB}$	Coremark run current in high performance mode	Executed from internal MRAM, cache enabled, SIMO buck enabled, core clock/HFRC=250 MHz, 128 kB TCM enabled, radio subsystem off	1.8	-	46.3	-	µW/ MHz
I_{SS1}	System Sleep mode 1 current - 128 kB TCM retained	WFI instruction with SLEEPDEEP=1, all core & peripheral clocks gated, HFRC on, XTAL off, SIMO buck enabled, NVM in standby, no System SRAM bank enabled/retained, cache enabled/retained, 128 kB TCM enabled/retained, radio subsystem off	1.8	-	582.3	-	µW
$I_{SDS2-128RET}$	System Deep Sleep mode 2 current - 128 kB TCM retained	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM in retention, cache retained, 128 kB TCM retained, radio subsystem off	1.8	-	18.8	-	µW
$I_{SDS2-2048RET}$	System Deep Sleep mode 2 current - 2048 kB TCM retained	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM in retention, cache retained, 1792 kB SSRAM + 256 kB TCM retained, radio subsystem off	1.8	-	34.8	-	µW
$I_{SDS3-128RET}$	System Deep Sleep mode 3 current - 128 kB TCM retained	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM in retention, cache retained, 128 kB TCM retained, radio subsystem off	1.8	-	9.0	-	µW
$I_{SDS3-2048RET}$	System Deep Sleep mode 3 current - all 2048 kB SRAM/ TCM retained	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM in retention, cache retained, 1792 kB SSRAM + 256 kB TCM retained, radio subsystem off	1.8	-	25.7	-	µW
I_{SDS4}	System Deep Sleep mode 4 current	WFI instruction with SLEEPDEEP=1, LFRC on (HFRC and XTAL off), SIMO buck enabled, NVM powered down, all SSRAM/TCM/cache powered down (not retained), radio subsystem off.	1.8	-	6.7	-	µW

30.4 Power-On Reset (POR) and Brown-Out Detector (BOD)

Table 35: Power-On Reset (POR) and Brown-Out Detector (BOD)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR_RISING}	POR rising threshold voltage	-	1.635 - 1.675	-	V
$V_{BODL\_FALLING}$	Brownout detection low falling threshold voltage	-	1.63 - 1.70	-	V

30.5 Resets

Table 36: Resets

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PU_{RST}	Internal nRST pull-up resistor		-	24	-	kΩ

30.6 General Purpose Input/Output (GPIO)

Table 37 contains specifications for the standard GPIO. Specifications for the High-Speed GPIO were not available at the time of release of this version of the datasheet.

Table 37: General Purpose Input/Output (GPIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Standard GPIOs[1]						
V_{OH}	High-level output voltage		0.8 x V_{DDHn}[2]	-	-	V
V_{OL}	Low-level output voltage		-	-	0.2 x V_{DDHn}	V
V_{IH}	Positive going input threshold voltage		0.7 x V_{DDHn}	-	-	V
V_{IL}	Negative going input threshold voltage		-	-	0.3 x V_{DDHn}	V
V_{HYS}	Input Hysteresis		0.12	0.14	0.16	V
C_{GPI}	Input capacitance		-	5	-	pF
I_{IN}	Input pin leakage current		-	1	20	nA
I_{INOD}	Open drain output leakage current		-	1	20	nA
R_{PD50K}	50 kΩ pull-down resistance, PULLCFG = 1	PULLCFG = 1	42.4	51.0	59.4	kΩ
R_{PU15K}	1.5 kΩ pull-up resistance, PULLCFG = 2	PULLCFG = 2	1.3	1.6	1.9	kΩ
R_{PU6K}	6 kΩ pull-up resistance, PULLCFG = 3	PULLCFG = 3	5.2	6.2	7.3	kΩ
R_{PU12K}	12 kΩ pull-up resistance, PULLCFG = 4	PULLCFG = 4	10.4	12.5	14.6	kΩ
R_{PU24K}	24 kΩ pull-up resistance, PULLCFG = 5	PULLCFG = 5	20.6	24.9	29.0	kΩ
R_{PU50K}	50 kΩ pull-up resistance, PULLCFG = 6	PULLCFG = 6	42.2	50.7	58.8	kΩ
R_{PU100K}	100 kΩ pull-up resistance, PULLCFG = 7	PULLCFG = 7	84.0	100.5	116.6	kΩ
I_{SRC_0p1DS}	Output source current, 0.1x drive strength	VDDHn = 1.8 V	3.1	3.8	4.8	mA
I_{SNK_0p1DS}	Output sink current, 0.1x drive strength	VDDHn = 1.8 V	3.5	4.5	6.0	mA
I_{SRC_0p5DS}	Output source current, 0.5x drive strength	VDDHn = 1.8 V	15.6	18.9	23.9	mA
I_{SNK_0p5DS}	Output sink current, 0.5x drive strength	VDDHn = 1.8 V	13.9	18.0	24.0	mA
I_{SRC_0p75DS}	Output source current, 0.75x drive strength	VDDHn = 1.8 V	25.0	30.3	38.3	mA
I_{SNK_0p75DS}	Output sink current, 0.75x drive strength	VDDHn = 1.8 V	20.8	27.0	35.9	mA

Table 37: General Purpose Input/Output (GPIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SRC_1p0DS}	Output source current, 1.0x drive strength	VDDHn = 1.8 V	31.2	37.8	47.8	mA
I_{SNK_1p0DS}	Output sink current, 1.0x drive strength	VDDHn = 1.8 V	27.8	36.0	47.9	mA
$T_{RISE\_STD\_0P1X}$	Rise time, 30 pF load, 0.1x drive strength, GPIOx	VDDHn = 1.8 V	-	11.9	-	ns
$T_{FALL\_STD\_0P1X}$	Fall time, 30 pF load, 0.1x drive strength, GPIOx	VDDHn = 1.8 V	-	9.3	-	ns
$T_{RISE\_STD\_0P5X}$	Rise time, 30 pF load, 0.5x drive strength, GPIOx	VDDHn = 1.8 V	-	2.4	-	ns
$T_{FALL\_STD\_0P5X}$	Fall time, 30 pF load, 0.5x drive strength, GPIOx	VDDHn = 1.8 V	-	2.5	-	ns
$T_{RISE\_STD\_0P75X}$	Rise time, 30 pF load, 0.75x drive strength, GPIOx	VDDHn = 1.8 V	-	1.6	-	ns
$T_{FALL\_STD\_0P75X}$	Fall time, 30 pF load, 0.75x drive strength, GPIOx	VDDHn = 1.8 V	-	1.7	-	ns
$T_{RISE\_STD\_1P0X}$	Rise time, 30 pF load, 1.0x drive strength, GPIOx	VDDHn = 1.8 V	-	1.3	-	ns
$T_{FALL\_STD\_1P0X}$	Fall time, 30 pF load, 1.0x drive strength, GPIOx	VDDHn = 1.8 V	-	1.3	-	ns
High-speed GPIOs:						
C_P	Parasitic capacitance[3]		-	-	3	pF

1. All GPIOs have Schmitt trigger inputs.
2. The designation “n” corresponds to the voltage source for the pin, e.g., VDDH1.
3. Spec is preliminary.

30.7 Clocks/Oscillators

Table 38: Primary Internal Clocks

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{HFRC_LP}	HFRC frequency - Low Power		-	96	-	MHz
F_{HFRC_HP1}	HFRC frequency - High Performance Burst Mode 1		-	192[1]	-	MHz
F_{HFRC_HP2}	HFRC frequency - High Performance Burst Mode 2		-	250	-	MHz
DC_{HFRC}	HFRC duty cycle		-	50	-	%
F_{LFRC}	LFRC frequency		-	887	-	Hz
DC_{LFRC}	LFRC duty cycle	CLKGEN_CLKOUT_CKSEL = LFRC_DIV2	-	50	-	%
F_{PLL_OUT}	System PLL output frequency[2]		1.22	-	250	MHz
$F_{PLL\_IN\_INT}$	System PLL input frequency - Integer Mode		1	-	48	MHz
$F_{PLL\_IN\_FRAC}$	System PLL input frequency - Fractional Mode		10	-	48	MHz
$ACC_{PLL\_OUT\_FRAC}$	System PLL output accuracy - Fractional Mode		-	24	-	bit
$Jitter_{PLL\_OUT\_INT}$	Maximum integrated jitter (10 kHz to Nyquist) - Integer Mode[3]		-	-	15	ps
$Jitter_{PLL\_OUT\_FRAC}$	Maximum integrated jitter (10 kHz to Nyquist) - Fractional Mode[1]		-	-	30	ps

1. The HFRC oscillator frequency is used to supply the 192 MHz HFRC_HP clock and is divided by 2 to provide the 96 MHz HFRC_LP clock.
2. The maximum clock for PLLPOSTDIV is 100 MHz while it is 250 MHz for PLLVCO.
3. This is PLL jitter only and actual jitter seen on clock sinks, either internal or external, will be higher as it includes the jitter added by clocks routings.

Table 39: Low-Frequency Crystal Oscillator

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{XT}	XT frequency		-	32.768	-	kHz
DC_{XT}	XT duty cycle		50	56	60	%
ΔFXTAL	Frequency tolerance[1]	Untrimmed; include initial tolerance/aging/ temperature drift	-50	-	50	PPM
ESR	Equivalent serial resistance		-	-	90	KΩ
$C_{EXT\_XT\_LOAD}$	Allowed external XI/XO load capacitance per pin[2]		-	-	10	pF

1. Recommended to achieve target internal clock frequencies which use the XTAL as reference clock
2. If oscillator allowance (≥ 4x) is insufficient after adding the load caps, the XTALGENCTRL_XTALBIASTRIM field value in MCUCTRL can be increased to help increase the allowance. Default value for this field is 0x38 and can be increased as high as 0x3F (about a 12% increase in bias current).

Table 40: High-Speed Crystal Oscillator

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{XTAL}	Crystal frequency		-	48	-	MHz
ΔFXTAL	Frequency tolerance	Untrimmed; include initial tolerance/aging/ temperature drift	-	-	±40	PPM
ESR	Equivalent serial resistance		20	-	80	Ω
T_{XTAL}	Startup time		-	1	-	ms
C_{XTAL_LOAD}	Crystal load capacitance		4	6	10	pF

NOTE

Load capacitors are integrated within the SoC, but it is recommended to keep pads available on the PCB design in case additional tuning is required. These capacitor pads do not have to be populated.

30.8 Counter/Timer (TIMER)

Table 41: Timer (TIMER)

Symbol	Parameter	Min	Typ	Max	Unit
F_{TIMER}	Input frequency	-	-	48	MHz

30.9 Radio Subsystem

The following specifications are applicable to the Apollo510B Lite SoC and Apollo510D Lite SoC.

Table 42: General Transmitter Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{OUT(MIN)}$	Minimum output power	Minimum Tx output power setting @ 1.8 V	-	-20	-	dBm
$P_{OUT(MAX)}$	Maximum output power	Maximum Tx output power setting @ 1.8 V	-	13	-	dBm
$P_{OUT\_CH\_VAR}$	Maximum Tx output variability between channels		-	-	0.5	dB
$P_{OUT\_AT\_-20P0}$ $P_{OUT\_AT\_-16p0}$ $P_{OUT\_AT\_-10p0}$ $P_{OUT\_AT\_-6p0}$ $P_{OUT\_AT\_0p0}$ $P_{OUT\_AT\_+5p0}$ $P_{OUT\_AT\_+6p0}$ $P_{OUT\_AT\_+13p0}$	Mean Tx output power	Mean Tx output power at -20.0 dBm Mean Tx output power at -16.0 dBm Mean Tx output power at -10.0 dBm Mean Tx output power at -6.0 dBm Mean Tx output power at 0.0 dBm Mean Tx output power at +5.0 dBm Mean Tx output power at +6.0 dBm Mean Tx output power at +13.0 dBm	-	-19.5 -17.1 -11.0 -6.8 -0.6 +5.0 +6.3 +12.9	-	dBm
P_{OUT_+D2}	Second harmonic output power level	Radio Tx at +10 dBm	-	-27	-	dBm
P_{OUT_+D3}	Third harmonic output power level	Radio Tx at +10 dBm	-	-23	-	dBm
P_{OUT_+D4}	Fourth harmonic output power level	Radio Tx at +10 dBm	-	-35	-	dBm
IMP_{RF}	RFIO impedance		-	50	-	ohms

Table 43: General Receiver Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{MAX\_RCVR\_INPUT}$	Maximum receiver input power	PER < 30.8%	-	0	-	dBm
$C/I_{co\text{-}channel}$	BLE Co-channel interference	Wanted signal at -67 dBm, modulated interferer in channel, PER < 30.8%	-	4	-	dB
$C/I_{co\text{-}channel}$	BR Co-channel interference	Wanted signal at -67 dBm, modulated interferer in channel, PER < 30.8%	-	5.8	-	dB
$C/I_{co\text{-}channel}$	EDR 2 Mbps Co-channel interference	Wanted signal at -67 dBm, modulated interferer in channel, PER < 30.8%	-	9	-	dB
$C/I_{co\text{-}channel}$	EDR 3 Mbps Co-channel interference	Wanted signal at -67 dBm, modulated interferer in channel, PER < 30.8%	-	14.8	-	dB
f_{ET}	Receiver frequency error tolerance		-75	+15 / -35	75	kHz

Table 44: BLE Receiver Sensitivity

Symbol	Parameter[1]	Conditions[2]	Min	Typ	Max	Unit
$RSENS_{CH\_VAR}$	Receiver sensitivity variance between channels	Except BLE channel 23.	-	±0.5	-	dB
$BLE\_RSENS_{2M\_37}$	BLE sensitivity @ 2 Mbps BLE ideal transmitter, <=37 bytes	All except Ch 23: Ch 23:	-	-94 -94	-	dBm
$BLE\_RSENS_{2M\_251}$	BLE sensitivity @ 2 Mbps BLE ideal transmitter, extended packet size = 251 bytes	All except Ch 23: Ch 23:	-	-93 -93	-	dBm
$BLE\_RSENS_{1M\_37}$	BLE sensitivity @ 1 Mbps BLE ideal transmitter, <=37 bytes	All except Ch 23: Ch 23:	-	-97 -96	-	dBm
$BLE\_RSENS_{1M\_251}$	BLE sensitivity @ 1 Mbps BLE ideal transmitter, extended packet size = 251 bytes	All except Ch 23: Ch 23:	-	-96 -94	-	dBm
$BLE\_RSENS_{500k\_37}$	BLE sensitivity @ 500 kbps BLE ideal transmitter, <=37 bytes	All except Ch 23: Ch 23:	-	-98 -98	-	dBm
$BLE\_RSENS_{500k\_251}$	BLE sensitivity @ 500 kbps BLE ideal transmitter, extended packet size = 251 bytes	All except Ch 23: Ch 23:	-	-97 -97	-	dBm
$BLE\_RSENS_{125k\_37}$	BLE sensitivity @ 125 kbps BLE ideal transmitter, <=37 bytes	All except Ch 23: Ch 23:	-	-104 -101	-	dBm
$BLE\_RSENS_{125k\_251}$	BLE sensitivity @ 125 kbps BLE ideal transmitter, extended packet size = 251 bytes	All except Ch 23: Ch 23:	-	-103 -100	-	dBm

1. BLE Channel 23 (2448 MHz) receiver sensitivity is reduced due to high-frequency crystal harmonics and is therefore specified separately from the other channels. Furthermore, channel 23 sensitivities under the given sets of conditions have a wider range than the other channels and can be as low as -87 dBm.
2. For all BLE receiver sensitivity specifications, the following common conditions apply: **PER < 30.8%, 27C, VDDP = 1.8 V**.

Table 45: Bluetooth Classic Receiver Sensitivity

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$RSENS_{CH\_VAR}$	Receiver sensitivity variance between channels	Except Bluetooth Classic channel 46.	-	±0.5	-	dB
$BTC\_RSENS_{2M\_37}$	Bluetooth Classic sensitivity @ 1 Mbps Basic Data Rate (DPSK), <=37 bytes	All except Ch 46: Ch 46:	-	-95 -91	-	dBm
$BTC\_RSENS_{1M\_37}$	Bluetooth Classic sensitivity @ 2 Mbps Enhanced Data Rate (/4 DPSK), <=37 bytes	All except Ch 46: Ch 46:	-	-92 -88	-	dBm
$BTC\_RSENS_{3M\_37}$	Bluetooth Classic sensitivity @ 3 Mbps Enhanced Data Rate (8-DPSK), <=37 bytes	All except Ch 46: Ch 46:	-	-87 -83	-	dBm

1. For all Bluetooth Classic receiver sensitivity specifications, the following common conditions apply: **BER < 0.1%, Buck En at 27C, VDDP = 1.8 V**.

30.10 General Purpose Analog-to-Digital Converter (ADC)

Table 46: Analog-to-Digital Converter (ADC)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{ADCCLK}	ADC Clock Frequency		-	24/48	-	MHz
ANALOG INPUT						
V_{ADCINN}	Maximum safe Input voltage range		0	-	VDDH	V
V_{ADCREF}	Internal reference voltage range		1.15	1.19	1.24	V
C_{ADCIN}	Input source capacitance		-	2	-	pF
SAMPLING DYNAMICS						
RES	Resolution		8	-	12	bit
F_{ADCONV}	Conversion rate[1]		-	2.0 (12 b) 2.4 (10 b) 2.8 (8 b)	-	MS/s
TTRIG_W-START_LP1_REF0	Delay from warm start trigger to start of scan, LPMODE1	LPMODE1	-	57	-	µs
TTRIG_W-START_LP0_REF0	Delay from warm start trigger to start of scan, LPMODE0	LPMODE0	-	<100	-	ns
TSNGLSLOT_SCNC-MP_PM12	Delay from scan start to scan complete, precision mode 12	Precision Mode 12	-	24	-	cycles
TSNGLSLOT_SCNC-MP_PM10	Delay from scan start to scan complete, precision mode 10	Precision Mode 10	-	20	-	cycles
TSNGLSLOT_SCNC-MP_PM8	Delay from scan start to scan complete, precision mode 8	Precision Mode 8	-	17	-	cycles
DYNAMIC CHARACTERISTICS, Internal 2.0 V Reference (Buck Mode, Single Ended Input, 1 kHz Input, ADC Running in 12-bit Mode)						
ENOB	Effective number of bits	1.8V	-	9.45	-	ENOB
THD_{ADC}	Total harmonic distortion (THD) - 1st 7 harmonics	1.8V	-	-71	-	dB
SNR_{ADC}	Signal-to-noise ratio (SNR)	1.8V	-	58.9	-	dB
$SFDR_{ADC}$	Spurious-free dynamic range (SFDR)	1.8V	-	74.2	-	dB
$SINAD_{ADC}$	Signal-to-noise and distortion ratio (SINAD)	1.8V	-	58.7	-	dB
PERFORMANCE						
NMC_{ADC}	Number of missing codes		-	0	-	Codes
INL_{ADC}	Integral nonlinearity	Full input range	-	± 3.5	-	LSB
DNL_{ADC}	Differential nonlinearity	Full input range	-	[-0.98, 2.2]	-	LSB
E_{ADC_OFFSET}	Offset error		-1	-	1	%FS
E_{ADC_GAIN}	Gain error		-2	-	2	%FS

Table 46: Analog-to-Digital Converter (ADC)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
INTERNAL TEMPERATURE SENSOR						
E_{TEMP}	Temperature sensor accuracy	10-bit resolution	-	± 3.5	-	°C
S_{TEMP}	Temperature sensor slope		-	3.229	-	mV/°C
BATTERY VOLTAGE MEASUREMENT						
$V_{BATTDIV}$	Battery divider voltage		0.342 * VDDH	0.349 * VDDH	0.357 * VDDH	V

1. Refer to Errata List for any known device issues which may impact the achievable conversion rate.

30.11 Display Controller (DC)

30.11.1 DC QSPI/SPI Interface

Timing characteristics have been determined by measurements on chip.

Table 47: DC QSPI/SPI Timing[1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$F_{SCLK(OUT)}$	SCLK OUT frequency		-	-	48[2]	MHz
$T_{LOW(SCLK)}$	Clock low time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS = 1.0x, 30 pF load	-	2	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS = 1.0x, 30 pF load	-	2	-	ns
$T_{SETUP(IN)}$	Data input data setup time		40	-	-	ns
$T_{HOLD(in)}$	Data input data hold time		1	-	-	ns
$T_{HOLD(OUT)}$	Data output data hold time		-1	-	-	ns
$T_{VALID(OUT)}$	Data output data valid time	DS = 1.0x, 30 pF load	-	-	5	ns

1. The CE pin is assumed to be controlled by SW.
2. Max clock frequency setting using HFRC clock source. Note that the specified $T_{VALID(OUT)}$ time of 5 ns exceeds a half cycle of 96 MHz clock. If the external SPI peripheral supports full-cycle data capture, then a 96 MHz clock is supported provided it can meet the hold time requirement with the $T_{HOLD(OUT)}$ of -1ns. It is recommended that customers perform compliance testing in their systems to ensure reliable operation.

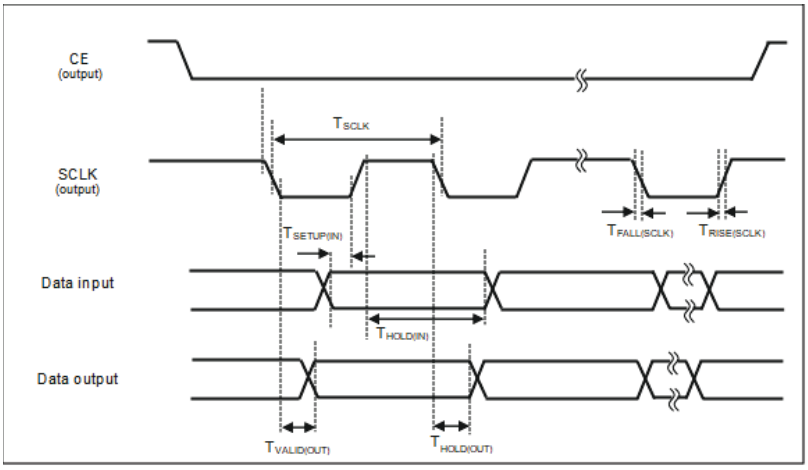


Figure 65. DC QSPI/SPI Timing Diagram

30.12 Multi-bit Serial Peripheral Interface (MSPI)

For MSPI0, MSPI1 and MSPI2 timings, the specifications cover nominal 1.8 V operation only.

Timing characteristics for the Apollo510 Lite SoC have been derived through simulations except where noted.

Table 48: MSPI General Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{DLY\_STEP\_SIZE}$	DDR Delay Step Size		80	-	200	ps

30.12.1 Standard 4-Wire Serial Mode - All MSPIs

For Standard 4-Wire Serial SPI Manager Mode, the following timing specifications assume that the MSPI is configured to use the same SCLK edge to launch MOSI and to capture MISO. This allows maximum speed to be achieved in serial SPI mode. If the MSPI is configured to follow the standard SPI timing mode, using a different SCLK edge to launch MOSI and to capture MISO, the setup and hold times of MISO is the same, but now with respect to the configured SCLK capture edge.

Timing characteristics have been determined through simulations.

Table 49: 4-Wire Serial Mode Timing (All MSPIs)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	48	MHz
T_{SCLK_LO}	Clock low time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load, GPIO Drive Strength=0.5x	-	1.0/1.5	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load, GPIO Drive Strength=0.5x	-	1.0/1.5	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$3.0/F_{SCLK}$	s
$T_{SETUP(MISO)}$	MISO/Data input setup time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	6.5	-	-	ns
$T_{HOLD(MISO)}$	MISO/Data input hold time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	0	-	-	ns
$T_{HOLD(MOSI)}$	MOSI/Data output hold time	15 pF Load, GPIO Drive Strength=0.5x	-2.0	-	-	ns
$T_{VALID(MOSI)}$	MOSI/Data output valid time	15 pF Load, GPIO Drive Strength=0.5x	-	-	2.5	ns

1. Turnaround set per memory target specification.

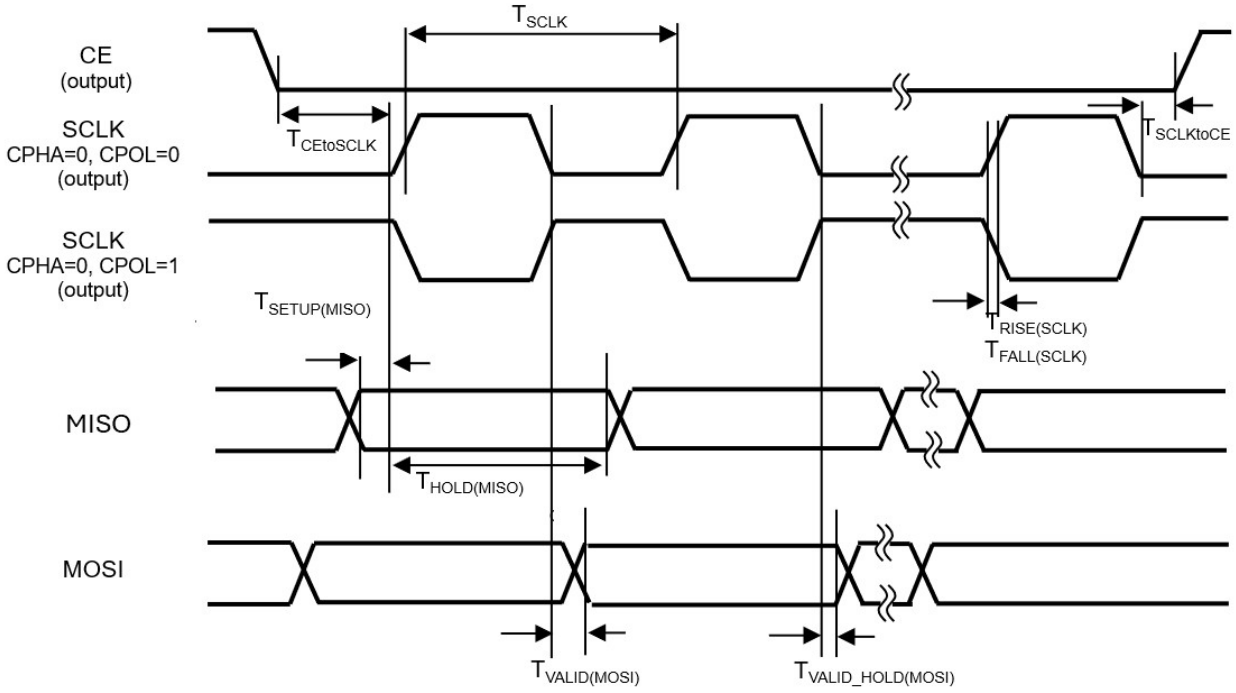


Figure 66. Standard 4-Wire Mode Timing Diagram, CPHA=0 (All MSPIs)

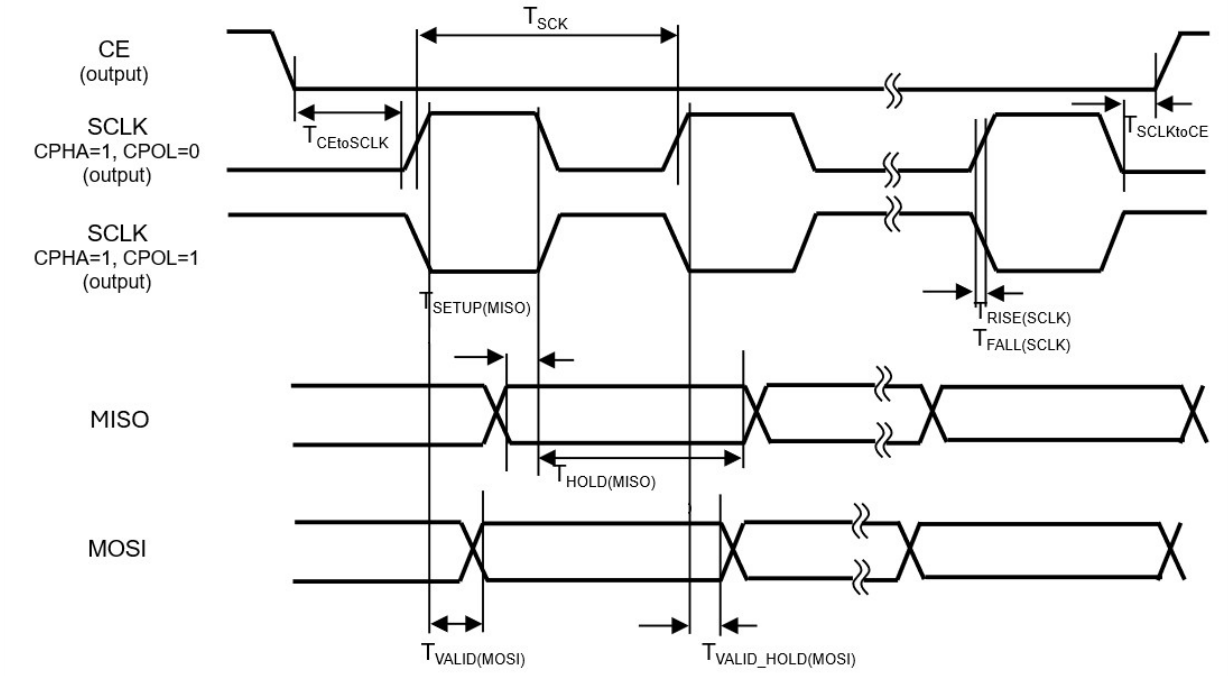


Figure 67. Standard 4-Wire Mode Timing Diagram, CPHA=1 (All MSPIs)

30.12.2 SDR Non-DQS SPI Modes - MSPI0 and MSPI2

For SDR Non-DQS Mode on MSPI0 and MSPI2 (non-skinny pads - See 30.12.3), the following specifications cover HexSPI (x16), OctalSPI (x8), and QuadSPI (x4) data widths. To use on-chip RX delay lines, the external data skew needs to be less than or equal to 4.0 ns. Timing parameters are applicable for the MSPI's voltage rail as defined above.

Timing characteristics have been determined through simulations. In addition, MSPI DDR and SDR have been spot-checked in the lab under worst case PVT conditions.

Table 50: SDR Non-DQS Mode Timing (MSPI0 and MSPI2)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	96	MHz
T_{SCLK_LO}	Clock low time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load, GPIO Drive Strength=0.5x	-	1	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load, GPIO Drive Strength=0.5x	-	1	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$3.0/F_{SCLK}$	s
$T_{SETUP(IN)}$	MISO/Data input setup time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	3.4	-	-	ns
$T_{HOLD(IN)}$	MISO/Data input hold time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	0	-	-	ns
$T_{HOLD(OUT)}$	MOSI/Data output hold time	15 pF Load, GPIO Drive Strength=0.5x	-2.3	-	-	ns
$T_{VALID(OUT)}$	MOSI/Data output valid time	15 pF Load, GPIO Drive Strength=0.5x	-	-	2.0	ns

1. Turnaround set per memory target specification.

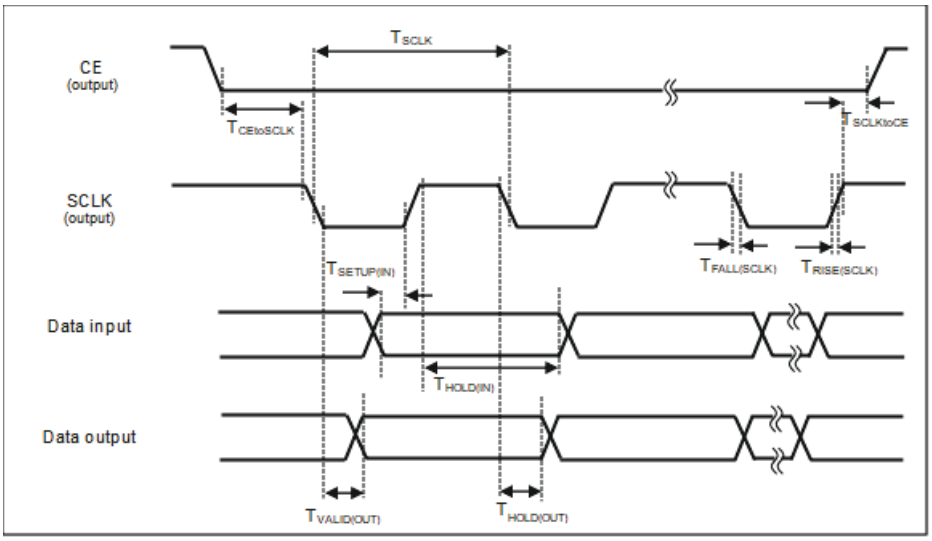


Figure 68. SDR Non-DQS Mode Timing Diagram (MSPI0 and MSPI2)

30.12.3 SDR Non-DQS SPI Modes - MSPI2 Skinny Pads

For SDR Non-DQS Mode on skinny pads offering MSPI2 pin functions (GPIO53-GPIO58), the following specifications cover QuadSPI (x4) data width. To use on-chip RX delay lines, the external data skew needs to be less than or equal to 4.0 ns. Timing parameters are applicable for the MSPI's voltage rail as defined above.

Timing characteristics have been determined through simulations. In addition, MSPI DDR and SDR have been spot-checked in the lab under worst case PVT conditions.

Table 51: SDR Non-DQS Mode Timing (MSPI2 - Skinny Pads)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	24	MHz
T_{SCLK_LO}	Clock low time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load, GPIO Drive Strength=0.5x	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load, GPIO Drive Strength=0.5x	-	2	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load, GPIO Drive Strength=0.5x	-	2	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load, GPIO Drive Strength=0.5x	$0.5/F_{SCLK}$	-	$3.0/F_{SCLK}$	s
$T_{SETUP(IN)}$	MISO/Data input setup time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	10	-	-	ns
$T_{HOLD(IN)}$	MISO/Data input hold time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	0	-	-	ns
$T_{HOLD(OUT)}$	MOSI/Data output hold time	15 pF Load, GPIO Drive Strength=0.5x	-2.0	-	-	ns
$T_{VALID(OUT)}$	MOSI/Data output valid time	15 pF Load, GPIO Drive Strength=0.5x	-	-	3.0	ns

1. Turnaround set per memory target specification.

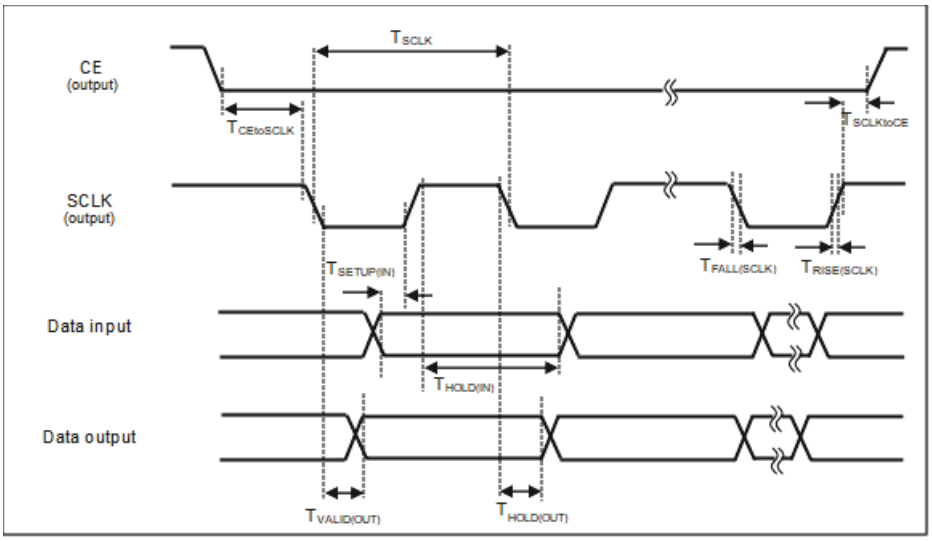


Figure 69. SDR Non-DQS Mode Timing Diagram (MSPI2 - Skinny Pads)

30.12.4 SDR Non-DQS SPI Modes - MSPI1

For SDR Non-DQS Mode on MSPI1, the following specifications cover QuadSPI (x4) data width. To use on-chip RX delay lines, the external data skew needs to be less than or equal to 4.0 ns. Timing parameters are applicable for the MSPI's voltage rail as defined above.

Timing characteristics have been determined through simulations. In addition, MSPI DDR and SDR have been spot-checked in the lab under worst case PVT conditions.

MSPI1 QuadSPI Mode Drive Strengths:

- CE: 0P5X, SR=0
- SCK: 0P5X, SR=0
- D0-D3: 1P0X, SR=0

Table 52: SDR Non-DQS Mode Timing (MSPI1)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	48	MHz
T_{SCLK_LO}	Clock low time	15 pF Load, GPIO Drive Strength=0.5x	0.45/F_{SCLK}	-	0.55/F_{SCLK}	s
T_{SCLK_HI}	Clock high time	15 pF Load, GPIO Drive Strength=0.5x	0.45/F_{SCLK}	-	0.55/F_{SCLK}	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load, GPIO Drive Strength=0.5x	-	1.5	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load, GPIO Drive Strength=0.5x	-	1.5	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load, GPIO Drive Strength=0.5x	0.5/F_{SCLK}	-	2.0/F_{SCLK}	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load, GPIO Drive Strength=0.5x	0.5/F_{SCLK}	-	3.0/F_{SCLK}	s
$T_{SETUP(IN)}$	MISO/Data input setup time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	5.5	-	-	ns
$T_{HOLD(IN)}$	MISO/Data input hold time	15 pF Load, GPIO Drive Strength=0.5x, TURNAROUND0=6, TXDQSDELAY0=3, RXDQSDELAY=6	0	-	-	ns
$T_{HOLD(OUT)}$	MOSI/Data output hold time	15 pF Load, GPIO Drive Strength=0.5x	-2.3	-	-	ns
$T_{VALID(OUT)}$	MOSI/Data output valid time	15 pF Load, GPIO Drive Strength=0.5x	-	-	2.5	ns

1. Turnaround set per memory target specification.

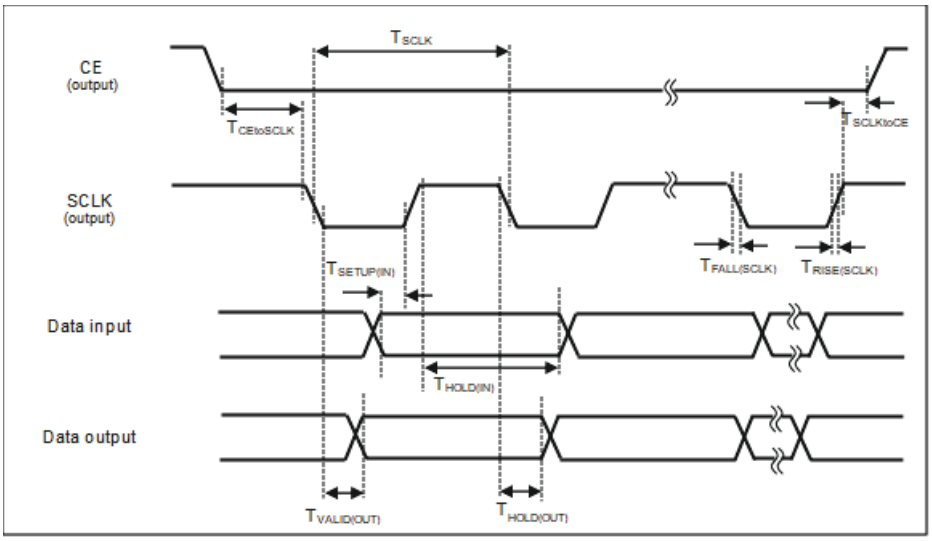


Figure 70. SDR Non-DQS Mode Timing Diagram (MSPI1)

30.12.5 MSPI0/MSPI2 DDR with DQS Mode (All Supported Data Widths)

The following specifications for MSPI0 and MSPI2 cover all supported data widths from QuadSPI (x4) up to HexSPI (x16).

To use on-chip RX delay lines, the external data skew needs to be less than or equal to 1.6 ns.

Timing parameters are applicable to 1.8 V nominal I/O voltage.

Timing characteristics have been determined through simulations. In addition, MSPI DDR and SDR have been spot-checked in the lab under worst case PVT conditions.

MSPI0 HexSPI Mode Drive Strengths:

- CE: 0P5X, LDRV=0
- SCK: 1P0X, LDRV=1
- D0-D15: 0P75X, LDRV=1

MSPI0/MSPI2 OctalSPI Mode Drive Strengths:

- CE: 0P5X, LDRV=0
- SCK: 1P0X, LDRV=1
- D0-D7: 0P75X, LDRV=1

Table 53: MSPI0/MSPI2 Timing - DDR with DQS Mode

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	125	MHz
T_{SCLK_LO}	Clock low time	15 pF Load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load	-	1	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load	-	1	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load,	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SETUP(IN)}$	Data input setup time	15 pF Load HexSPI: TURNAROUND0=14, TXDQS-DLY=0, RXDQSDLY=4 OctalSPI: TURNAROUND0=10, TXDQS-DLY=0, RXDQSDLY=14	1.5	-	-	ns
$T_{HOLD(IN)}$	Data input hold time	15 pF Load HexSPI: TURNAROUND0=14, TXDQS-DLY=0, RXDQSDLY=4 OctalSPI: TURNAROUND0=10, TXDQS-DLY=0, RXDQSDLY=14	2.5	-	-	ns
$T_{HOLD(OUT)}$	Data output hold time	15 pF Load	$(0.225/F_{SCLK}) - 0.9(10)^{-9}$	-	-	s
$T_{VALID(OUT)}$	Data output valid time	15 pF Load	-	-	$(0.275/F_{SCLK}) + 0.9(10)^{-9}$	s

1. Turnaround set per memory target specification. RXDQS/TXDQS delay values determined by timing scan. See AmbiqSuite SDK for more details.

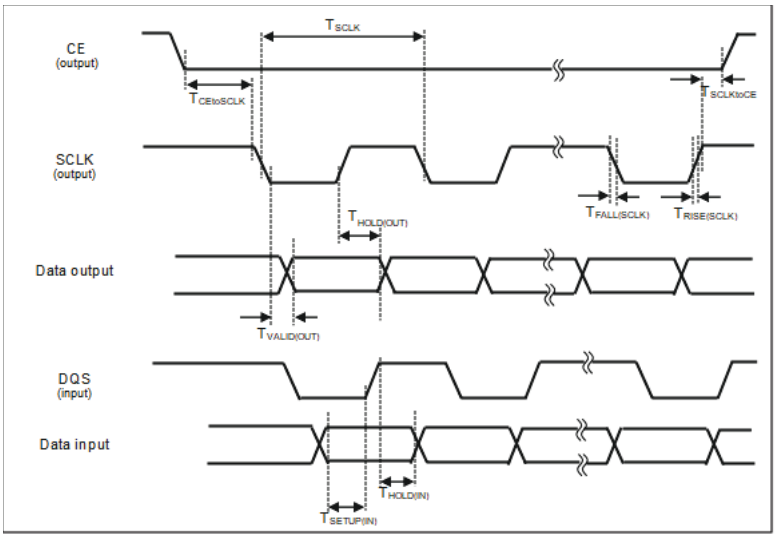


Figure 71. MSPI0/MSPI2 DDR with DQS Mode Timing Diagram

30.12.6 MSPI1 DDR with DQS Mode (Supported Data Width)

The following specifications for MSPI1 cover QuadSPI (x4) data width.

To use on-chip RX delay lines, the external data skew needs to be less than or equal to 4.0 ns.

Timing parameters are applicable to 1.8 V nominal I/O voltage for MSPI1.

Timing characteristics have been determined through simulations. In addition, MSPI DDR and SDR have been spot-checked in the lab under worst case PVT conditions.

MSPI1 QuadSPI Mode Drive Strengths:

- CE: 0P5X, SR=0
- SCK: 0P5X, SR=0
- D0-D3: 1P0X, SR=0

Table 54: MSPI1 Timing - DDR with DQS Mode

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency range		-	-	48	MHz
T_{SCLK_LO}	Clock low time	15 pF Load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
T_{SCLK_HI}	Clock high time	15 pF Load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	15 pF Load	-	1.5	-	ns
$T_{FALL(SCLK)}$	Clock fall time	15 pF Load	-	1.5	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	15 pF Load	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	15 pF Load	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SETUP(IN)}$	Data input setup time	15 pF Load, TURNAROUND0=6, TXDQSDELAY0=WS[2], RXDQSDELAY=WS	1.5	-	-	ns
$T_{HOLD(IN)}$	Data input hold time		2.5	-	-	ns
$T_{HOLD(OUT)}$	Data output hold time	15 pF Load	$(0.225/F_{SCLK}) - 0.3(10)^{-9}$	-	-	s
$T_{VALID(OUT)}$	Data output valid time	15 pF Load	-	-	$(0.275/F_{SCLK}) + 2.9(10)^{-9}$	s

1. Turnaround set per memory target specification.
2. WS = Window Scanned

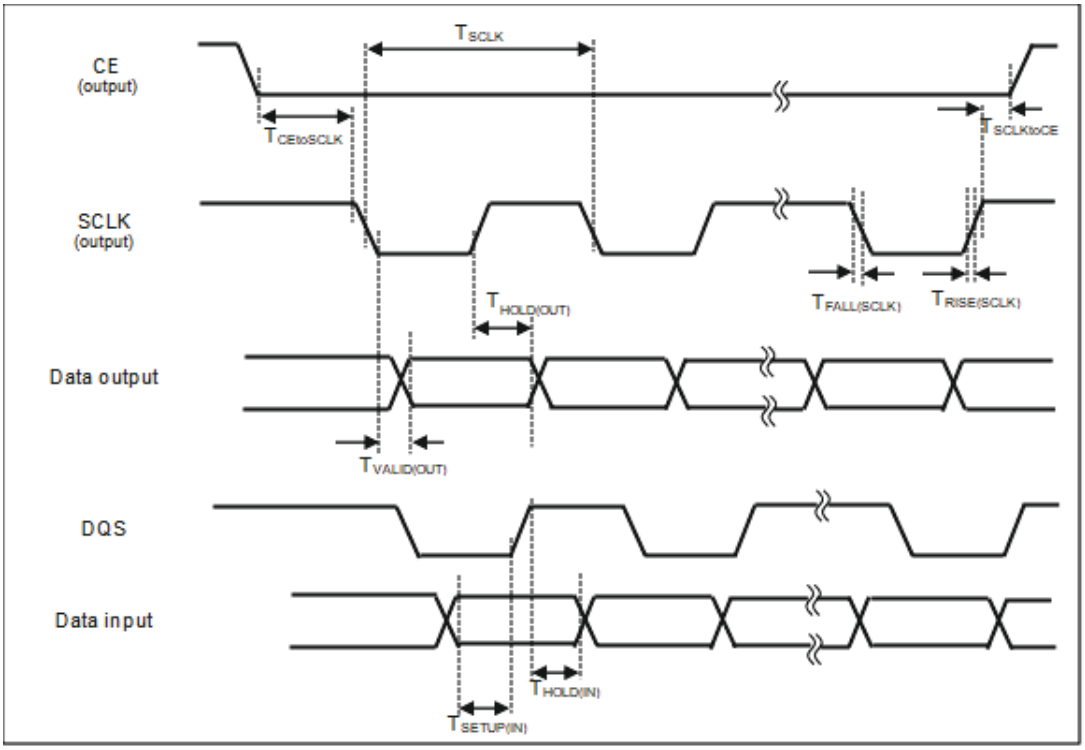


Figure 72. MSPI1 DDR with DQS Mode Timing Diagram

30.13 I2C/SPI Manager (IOM)

30.13.1 Inter-Integrated Circuit (I2C) Interface

Table 55: I2C Interface Timing

Symbol	Parameter	VCC	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	1.71 V - 2.2 V	10	-	1000	kHz
t_{LOW}	Low period of SCL clock	1.71 V - 2.2 V	1.3	-	-	µs
t_{HIGH}	High period of SCL clock	1.71 V - 2.2 V	600	-	-	ns
t_{RISE}	Rise time of SDA and SCL	1.71 V - 2.2 V	-	-	300	ns
t_{FALL}	Fall time of SDA and SCL	1.71 V - 2.2 V	-	-	300	ns
$t_{HD:STA}$	START condition hold time	1.71 V - 2.2 V	600	-	-	ns
$t_{SU:STA}$	START condition setup time	1.71 V - 2.2 V	600	-	-	ns
$t_{SU:DAT}$	SDA setup time	1.71 V - 2.2 V	100	-	-	ns
$t_{HD:DAT}$	SDA hold time	1.71 V - 2.2 V	0	-	-	ns
$t_{SU:STO}$	STOP condition setup time	1.71 V - 2.2 V	600	-	-	ns
t_{BUF}	Bus free time before a new transmission	1.71 V - 2.2 V	1.3	-	-	µs

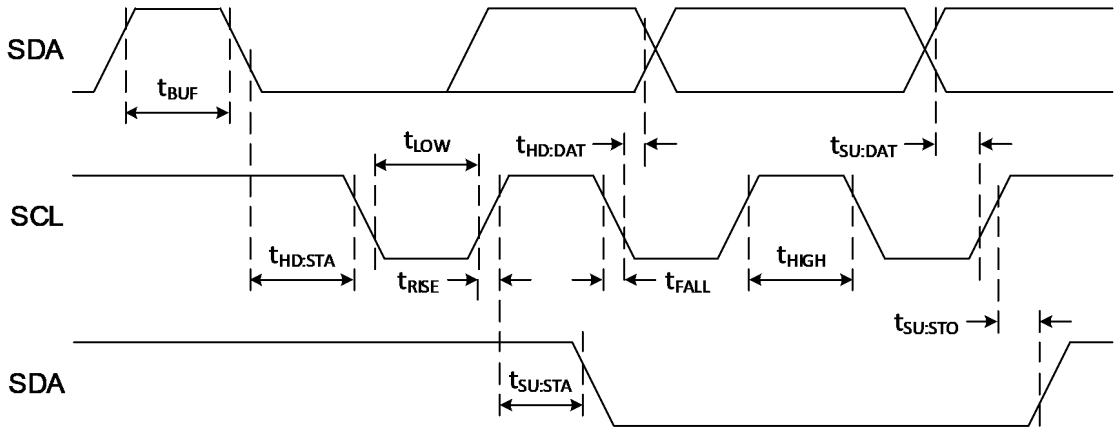


Figure 73. I2C Interface Timing Diagram

30.13.2 Serial Peripheral Interface (SPI) Manager Interface

Timing characteristics have been determined through simulations.

Table 56: SPI Manager Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} ($1/T_{SCLK}$)	SCLK frequency range	DS=0.5x, 30pF load	-	-	24	MHz
$F_{SCLK-3WIRE}$	SCLK frequency range - 3-wire mode	DS=0.5x, 30pF load	-	-	12	MHz
$T_{LOW(SCLK)}$	Clock low time	DS=0.5x, 30pF load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS=0.5x, 30pF load	$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS=0.5x, 30pF load	-	2	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS=0.5x, 30pF load	-	2	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge	DS=0.5x, 30pF load	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SCLKtoCE}$	Last SCLK to CE	DS=0.5x, 30pF load	$0.5/F_{SCLK}$	-	$2.0/F_{SCLK}$	s
$T_{SETUP\ (MISO)}$	MISO input data setup time	DS=0.5x, 30pF load	5.5	-	-	ns
$T_{HOLD\ (MISO)}$	MISO input data hold time	DS=0.5x, 30pF load	2	-	-	ns
$T_{SETUP\_3WIRE\ (MOSI\_IN)}$	MOSI input data setup time for 3-wire mode	DS=0.5x, 30pF load	34	-	-	ns
$T_{HOLD\_3WIRE\ (MOSI\_IN)}$	MOSI input data hold time for 3-wire mode	DS=0.5x, 30pF load	1	-	-	ns
$T_{VALID\_HOLD\ (MOSI)}$	MOSI output data hold time	DS=0.5x, 30pF load	-8.4	-	-	ns
$T_{VALID\ (MOSI)}$	MOSI output data valid time	DS=0.5x, 30pF load		-	10	ns
$T_{VALID\_HOLD\_3WIRE\ (MOSI)}$	MOSI output data hold time for 3-wire mode	DS=0.5x, 30pF load	-4	-	-	ns
$T_{VALID\_3WIRE\ (MOSI)}$	MOSI output data valid time for 3-wire mode	DS=0.5x, 30pF load	-	-	32	ns

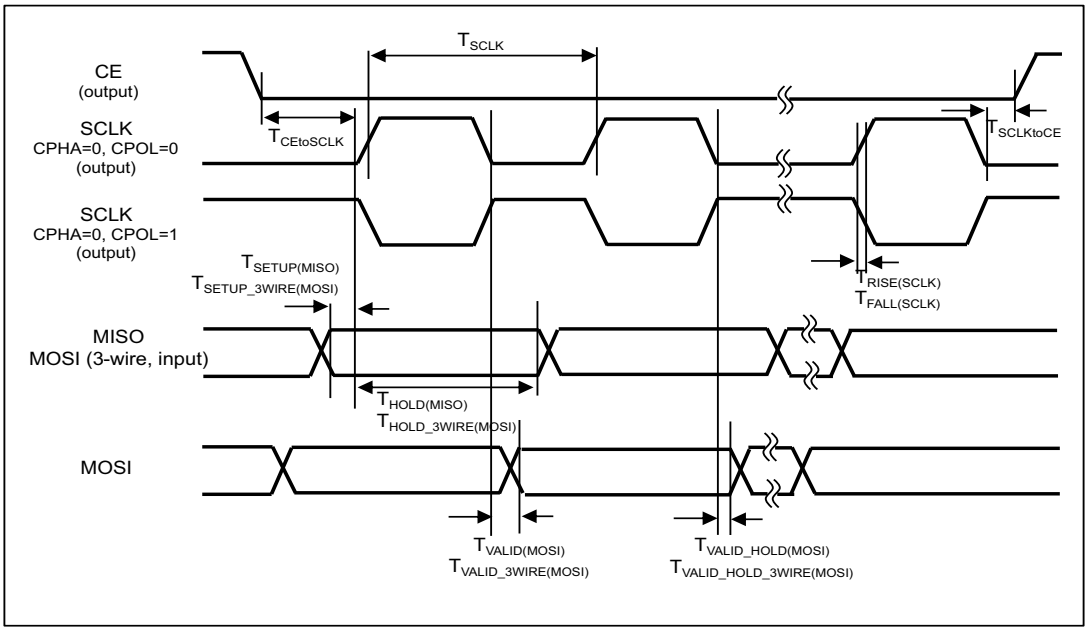


Figure 74. SPI Manager Interface Timing Diagram, CPHA = 0

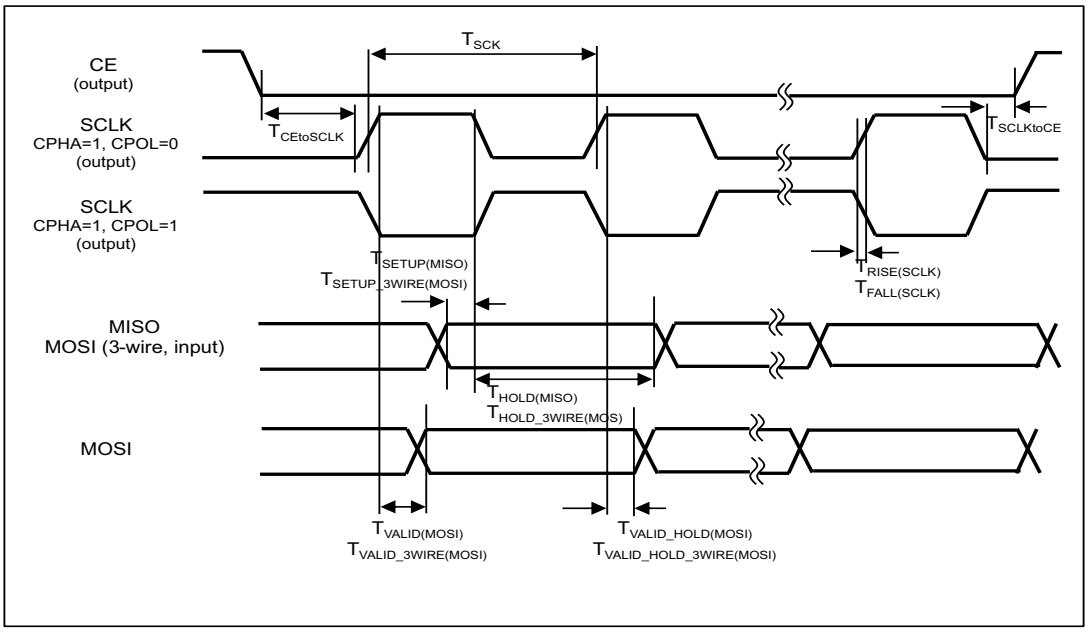


Figure 75. SPI Manager Interface Timing Diagram, CPHA = 1

30.14 Improved Inter-Integrated Circuit (I3C) Host

Table 57: I3C DC I/O Stage Specifications

Symbol	Parameter	Description	Min	Typ	Max	Units	Notes
VDDH2	Operating Voltage		1.71	1.8	1.95	V	1
V_{IL}	Low-Level Input Voltage		-0.1 x VDDH2	-	0.3 x VDDH2	V	6
V_{IH}	High-Level Input Voltage		0.7 x VDDH2	-	1.1 x VDDH2	V	6
V_{HYS}	Schmitt Trigger Inputs Hysteresis		0.1 x VDDH2	-		V	-
V_{OH}	Output High Level	IOH = -3 mA	-	-	VDDH2 – 0.27	V	2,7
V_{OL}	Output Low Level	IOL = 3 mA	-	-	0.27	V	7
Ci	Capacitance (per I/O Pin)	For < 1.8 V nominal	-	-	5	pF	4
		For ≥ 1.8 V nominal	-	-	10		
ΔC	Capacitance Mismatch Between Pins	Difference between SDA and SCL capacitance CI ≤ 5 pF	-	-	1.5	pF	4
		Difference between SDA and SCL capacitance CI > 5 pF	-	-	3		
Rp	Pull-Up for Open Drain	Pull up resistance in open drain mode	-	-	2833	Ω	3,5

Notes:

1. This specification considers only 1.8 V with associated tolerances. Other voltage levels within VDDH2's specified range are not prohibited. Any I3C bus implementation must ensure the correct operation of the devices resident on the bus, notably the inter-compatibility of their voltage ranges.
2. Negative sign for currents indicates that the device is sinking current in this condition.
3. Pull-up for open drain shall be switched off during I3C push-pull operation. May be implemented as:
   - A pull-up internally
   - A current source internally
   - An external pull-up resistor driven by a pin

   When I3C is powered off, a weak pull-up (~100kΩ) is applied to the SDA line (high-keeper pull-up requirements) of the I3C spec.
4. For devices that support both 1.8 V and 3.3 V, the larger capacitance may be used.
5. Open Drain never occurs on SCL.
6. The V_{IL} min and V_{IH} max allow for normal undershoot and overshoot on a Bus. Voltages that are lower than VIL min and higher than V_{IH} max will be handled by protection circuits (i.e., ESD protection) as with any GPIO or standard pad peripheral. The board designer should be made aware of any deviations outside VIL min and VIH max.
7. A device must be able to continuously sink the indicated current (indicated as a negative number) in this condition. For most pad types, the drive strength must be rated at twice the indicated current, since the rated drive strength is normally the peak current when the voltage difference is at its maximum. For V_{OL}, this is SDA at VDDH2; for V_{OH}, this is SDA at ground.

Table 58: Timing Parameters for HDR-TSP and HDR-TSL modes

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{EDGE}	Edge-to-Edge Period	t_{DIG_H}	-	-	ns	1
t_{SKEW}	Allowed Difference Between Signals for 'Simultaneous' Change	-	-	12.8	ns	-

Table 58: Timing Parameters for HDR-TSP and HDR-TSL modes

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{EYE}	Stable Condition Between Symbols	12	-	-	ns	-
t_{SYMBOL}	Time Between Successive Symbols	$t_{EDGE\ (Min)}$	-	-	ns	-
t_{CLOCK}	Symbol Clock	$1 / f_{SCL\ (Max)}$	-	-	-	-

Notes:

1. t_{DIG_H} is defined as “the minimum required high-level duration of the SCL clock signal as seen at the receiver”, per the full I3C v1.0 spec and the I3C basic v1.1.1 spec (section 6.2). For push-pull signaling, these are typically defined as 32 ns each, i.e., the clock must be high for at least 32 nanoseconds.

2.Edges occur at the rate of 1 / (t_{EDGE} x 2).

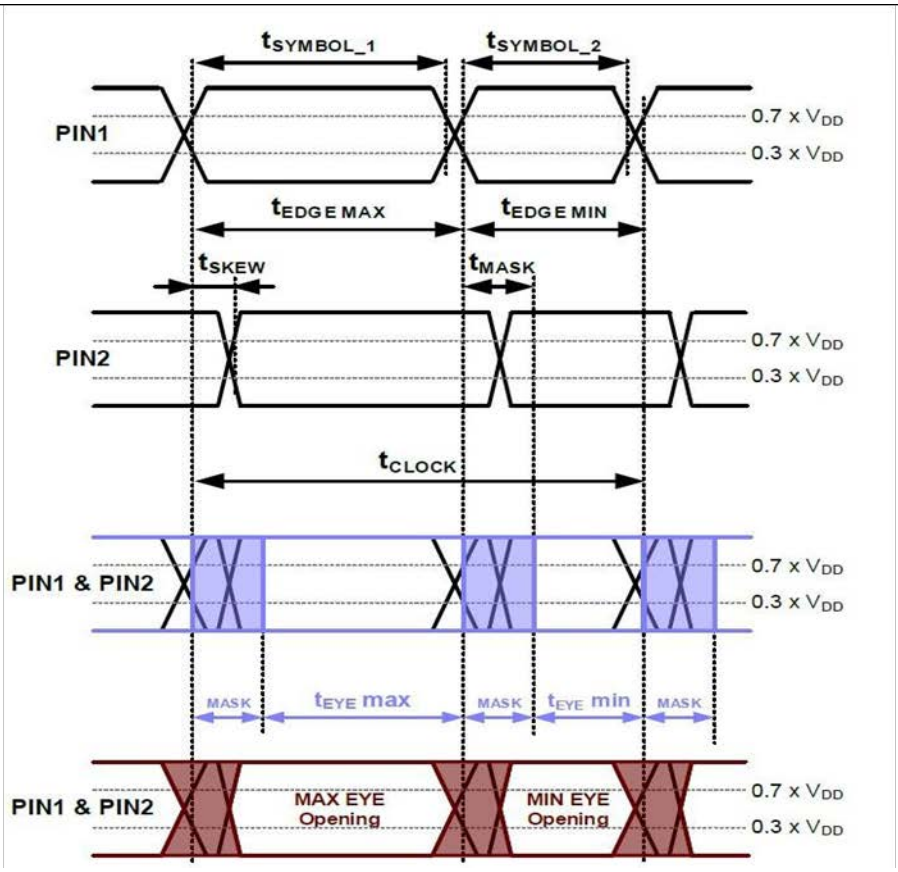


Figure 76. Ternary Protocol Timing Diagram

Notes:

1. V_{DD} is VDDH2 supply.

30.15 SPI Subordinate (IOSFD)

Timing characteristics have been determined by measurements on chip except for 3-wire mode timings which have been derived through simulation.

Table 59: SPI Subordinate Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} ($1/T_{SCLK}$)	SCLK frequency range		-	8	24[1]	MHz
$F_{SCLK-3WIRE}$	SCLK frequency range - 3-wire mode		-	8	12	MHz
$T_{LOW(SCLK)}$	Clock low time		$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time		$0.45/F_{SCLK}$	-	$0.55/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time		-	2	-	ns
$T_{FALL(SCLK)}$	Clock fall time		-	2	-	ns
$T_{CEtoSCLK}$	CE to first SCLK edge		18	-	-	ns
$T_{SCLKtoCE}$	Last SCLK to CE		18	-	-	ns
$T_{SETUP(MOSI)}$	MOSI input data setup time		4	-	-	ns
$T_{HOLD(MOSI)}$	MOSI input data hold time		3	-	-	ns
$T_{SETUP\_3WIRE(MOSI\_IN)}$	MOSI input data setup time for 3-wire mode		35	-	-	ns
$T_{HOLD\_3WIRE(MOSI\_IN)}$	MOSI input data hold time for 3-wire mode		3	-	-	ns
$T_{VALID\_HOLD(MISO)}$	MISO output data hold time	DS=0.5x, 15 pF Load	4	-	-	ns
$T_{VALID(MISO)}$	MISO output data valid time	DS=0.5x, 15 pF Load	-	-	15.5	ns
$T_{VALID\_HOLD\_3WIRE(MOSI)}$	MOSI output data hold time for 3-wire mode	DS=0.5x, 15 pF Load	4	-	-	ns
$T_{VALID\_3WIRE(MOSI)}$	MOSI output data valid time for 3-wire mode	DS=0.5x, 15 pF Load	-	-	32	ns

1. Due to the specified $T_{VALID(MISO)}$ time, max clock is restricted to 24 MHz. If the external SPI host supports full-cycle data capture, max clock is 48 MHz.

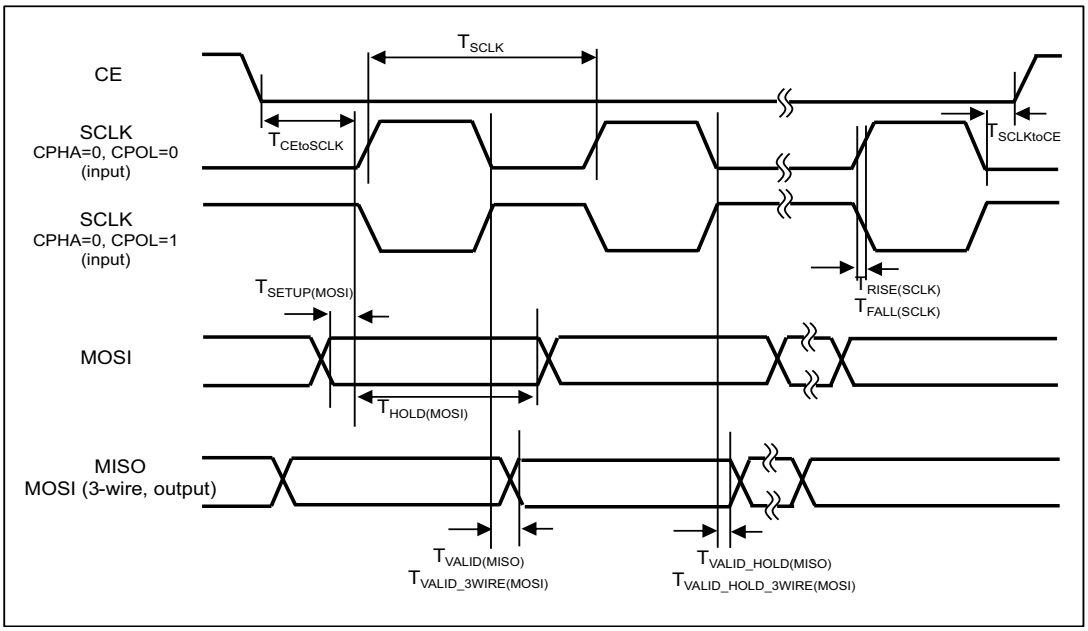


Figure 77. SPI Subordinate Interface Timing Diagram, CPHA = 0

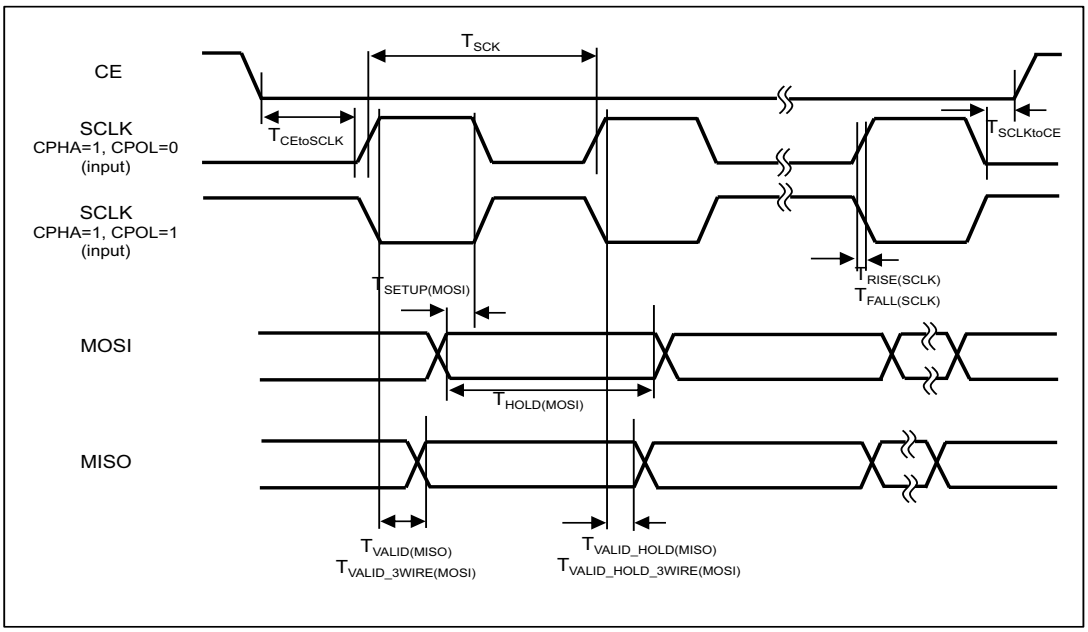


Figure 78. SPI Subordinate Interface Timing Diagram, CPHA = 1

30.16 Universal Asynchronous Receiver/Transmitter (UART)

Table 60: Universal Asynchronous Receiver/Transmitter (UART)

Symbol	Parameter	Min	Typ	Max	Unit
F_{BAUD}	UART baud rate	-	-	5.0	Mbps

30.17 Universal Serial Bus (USB)

30.17.1 USB Power Gating and Leakage Current

Table 61: USB Power Gating

VDDF_USB_SW	VDDUSB0P9	VDDUSB33	Requirements
OFF	ON	ON	This state may result in elevated leakage current (see USB Leakage Current table below) and is not recommended in a system where the 0.9 V rail is powered from the battery and not USB VBUS.
ON	OFF	ON	VDDUSB0P9 must be pulled to ground. A floating supply will cause leakage from VDDF_USB_SW.
ON	OFF	OFF	VDDUSB0P9 / VDDUSB33 must be pulled to ground. A floating supply will cause leakage from VDDF_USB_SW.
OFF	OFF	ON	VDDUSB0P9 must be pulled to ground. A floating supply will cause leakage from VDDUSB33.

NOTES:
1) The VDDF_USB_SW rail is internal, the VDDUSB33 rail is external, and the VDDUSB0P9 rail may be either external or internal on the Apollo510 Lite SoC. External rails are controlled in hardware while the internal rails are controlled through register settings.
2) Removal of VDDUSB33 while VDDUSB0P9 is still powered on is not supported as it will affect long term reliability of the PHY.

Table 62: USB Leakage Current

Operating Conditions	VDDF_USB_SW (0.8 V nominal)	VDDUSB0P9 (0.9 V nominal)	VDDUSB33 (3.3 V nominal)	Worst case leakage @ VDDF_USB_SW	Worst case leakage @ VDDUSB0P9	Worst case leakage @ VDDUSB33
USB comes out of reset; PHY is in suspend mode	0.8 V	0.9 V	3.3 V	0	4 µA	40 µA
PHY is not operational; All input signals are at their default values.	0.8 V	0	3.3 V	0	0	40 µA
PHY is not operational; All input signals are at their default values.	0	0	3.3 V	0	0	1.2 µA
PHY is not operational; All input signals are at their default values.	0	0.9 V	3.3 V	0	X	X

NOTES:
1) All numbers given are with the assumption PHY is brought to suspend state, and the USB controller is held in reset before any rails are powered off.
2) Both DP/DM are in the high-Z state if the PHY is powered off when in suspend or reset state. Otherwise, the DP/DM state depends on the state USB controller/SW is in at the moment when PHY power goes off.
3) Leakage via external ESD protection brings DP/DM voltage to zero when PHY puts them in the high-Z state.
4) If 3.3 V is always powered, the software must enable internal 0.8 V rail before the internal 0.9V. Otherwise, leakage can't be controlled (last two rows of the table).
5) "X" indicates that the leakage current is unpredictable and could be > 40 mA.
6) Assuming 3.3 V is always on, the power-on sequence depicted below is allowed with no limitations on the duration [t0...t1]. The leakage for the period from t0 to t1 is several microamps.
7) Powering down the VDDUSB33 rail with VDDUSB0P9 still active is not supported as it will affect long term reliability of the PHY. This is applicable for the Apollo510 Lite SoC only if an external 0.9 V power supply is used. The internal LDO is powered from VDDUSB33 (3.3 V) and therefore 0.9 V will be powered down automatically.

30.17.2 USB PHY Power and Interface Timing Requirements

Table 63: USB PHY Power Supply

Voltage Supply	Parameter	Condition	Min	Typ	Max	Units
VDDUSB33	Voltage		3.0	-	3.63	V
VDDUSB33	Current consumption	In functional FS/HS state	-	6.2	-	mA
VDDUSB0P9	Voltage		0.84	-	0.99	V
VDDUSB0P9	Ripple		-	-	5	%
VDDUSB0P9	Current consumption	In functional FS/HS state	-	23.2	40	mA
VDDUSB33	Current Consumption	In suspend state when both 3.3 V and 0.9 V are supplied.	-	-	4	µA
VDDUSB0P9	Current Consumption		-	-	5	µA

30.18 Secure Digital Input Output (SDIO)

Table 64: SDIO General Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TX\_DLY\_STEP\_SIZE}$	TX Delay Step Size		0.12	-	0.40	ns
$T_{RX\_DLY\_STEP\_SIZE}$	RX Delay Step Size		0.09	-	0.35	ns

30.18.1 SD SDR50 Mode Interface

Timing characteristics have been determined by measurements on chip.

The following specifications are with the settings MCUCTRL_SDIOnCTRL_SDIOnOTAPDLYSEL = 4 and MCUCTRL_SDIOnCTRL_SDIOnITAPDLYSEL = 8.

Table 65: SD SDR50 Mode Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{CLK} ($1/T_{CLK}$)	SCLK frequency range		-	-	96	MHz
T_{CLK_LO}	Clock low time	15 pF Load, DS=1.0x	$0.4/F_{CLK}$	-	$0.6/F_{CLK}$	s
T_{CLK_HI}	Clock high time	15 pF Load, DS=1.0x	$0.4/F_{CLK}$	-	$0.6/F_{CLK}$	s
$T_{RISE(CLK)}$	Clock rise time	15 pF Load, DS=1.0x	-	2	-	ns
$T_{FALL(CLK)}$	Clock fall time	15 pF Load, DS=1.0x	-	2	-	ns
$T_{SETUP(IN)}$	Data/CMD input setup time	15 pF Load, DS=1.0x	2	-	-	ns
$T_{HOLD(IN)}$	Data/CMD input hold time	15 pF Load, DS=1.0x	3	-	-	ns
$T_{HOLD(OUT)}$	Data/CMD output hold time	15 pF Load, DS=1.0x	2	-	-	ns
$T_{VALID(OUT)}$	Data/CMD output valid time	15 pF Load, DS=1.0x	-	-	7	ns

Note: Card specifications with respect to clock rise:

- Input setup/hold = 3 ns/0.8 ns
- Output min/max = 1.5 ns/7.5 ns

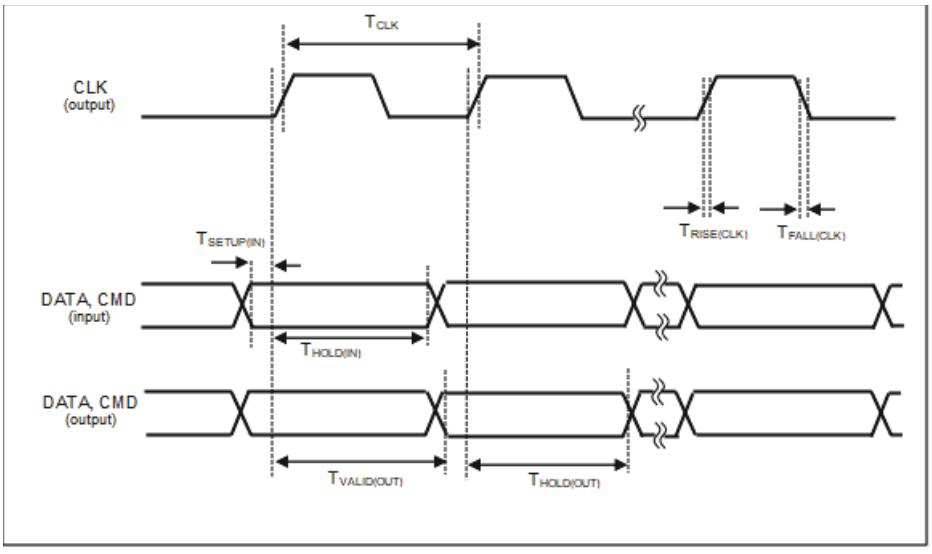


Figure 79. SD SDR50 Mode Interface Timing Diagram

30.18.2 SD DDR50 Mode Interface

Timing characteristics have been determined by measurements on chip.

The following specifications are with the settings MCUCTRL_SDIOnCTRL_SDIOnOTAPDLYSEL = 4 and MCUCTRL_SDIOnCTRL_SDIOnITAPDLYSEL = 8.

Table 66: SD DDR50 Mode Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{CLK} ($1/T_{CLK}$)	SCLK frequency range		-	-	48	MHz
T_{CLK_LO}	Clock low time	30 pF Load, DS=1.0x	$0.4/F_{CLK}$	-	$0.6/F_{CLK}$	s
T_{CLK_HI}	Clock high time	30 pF Load, DS=1.0x	$0.4/F_{CLK}$	-	$0.6/F_{CLK}$	s
$T_{RISE(CLK)}$	Clock rise time	30 pF Load, DS=1.0x	-	2	-	ns
$T_{FALL(CLK)}$	Clock fall time	30 pF Load, DS=1.0x	-	2	-	ns
$T_{SETUP(IN)}$	Data/CMD input setup time	30 pF Load, DS=1.0x	2	-	-	ns
$T_{HOLD(IN)}$	Data/CMD input hold time	30 pF Load, DS=1.0x	3	-	-	ns
$T_{HOLD(OUT)}$	Data/CMD output hold time	30 pF Load, DS=1.0x	1	-	-	ns
$T_{VALID(OUT)}$	Data/CMD output valid time	30 pF Load, DS=1.0x	-	-	7	ns

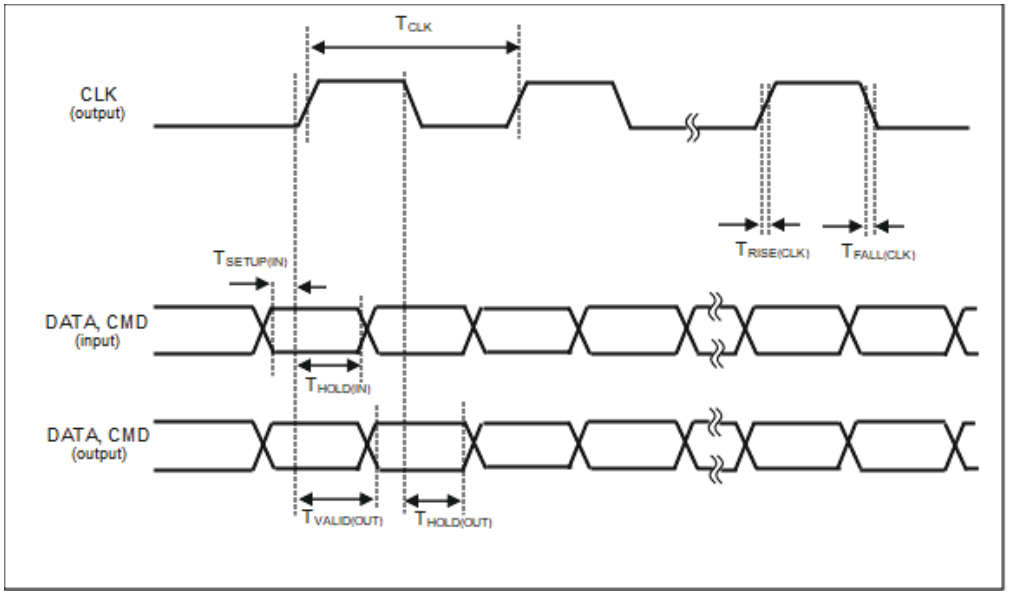


Figure 80. SD DDR50 Mode Interface Timing Diagram

30.19 Audio

30.19.1 I²S Interface

Timing characteristics have been determined by measurements on chip.

Table 67: I²S Subordinate Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} (1/TSCLK)	SCLK frequency range		-	-	12[1]	MHz
$T_{LOW(SCLK)}$	Clock low time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS = 1.0x, 30 pF load	-	2	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS = 1.0x, 30 pF load	-	2	-	ns
$T_{SETUP(WSIN)}$	WS input data setup time		8	-	-	ns
$T_{HOLD(WSIN)}$	WS input data hold time		9	-	-	ns
$T_{SETUP(SDIN)}$	SDIN input data setup time		8	-	-	ns
$T_{HOLD(SDIN)}$	SDIN input data hold time		9	-	-	ns
$T_{HOLD(SDOUT)}$	SDOUT output data hold time	DS = 1.0x, 30 pF load	4	-	-	ns
$T_{VALID(SDOUT)}$	SDOUT output data valid time	DS = 1.0x, 30 pF load	-	-	25	ns

1. Max frequency from 48 MHz RF_XTAL_HS clock source.

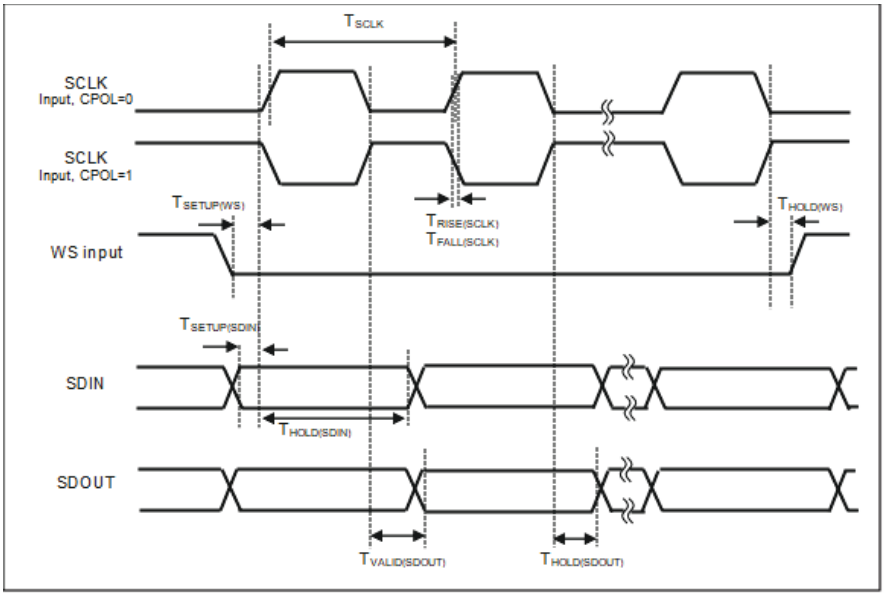


Figure 81. I²S Subordinate Interface Timing Diagram

Timing characteristics have been determined by measurements on chip.

Table 68: I²S Manager Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} (1/TSCLK)	SCLK frequency range		-	-	12[1]	MHz
$T_{LOW(SCLK)}$	Clock low time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{HIGH(SCLK)}$	Clock high time	DS = 1.0x, 30 pF load	$0.4/F_{SCLK}$	-	$0.6/F_{SCLK}$	s
$T_{RISE(SCLK)}$	Clock rise time	DS = 1.0x, 30 pF load	-	2	-	ns
$T_{FALL(SCLK)}$	Clock fall time	DS = 1.0x, 30 pF load	-	2	-	ns
$T_{HOLD(WSOUT)}$	WS output data hold time	DS = 1.0x, 30 pF load	4	-	-	ns
$T_{VALID(WSOUT)}$	WS output data valid time	DS = 1.0x, 30 pF load	-	-	25	ns
$T_{SETUP(SDIN)}$	SDIN input data setup time		8	-	-	ns
$T_{HOLD(SDIN)}$	SDIN input data hold time		9	-	-	ns
$T_{HOLD(SDOUT)}$	SDOUT output data hold time	DS = 1.0x, 30 pF load	4	-	-	ns
$T_{VALID(SDOUT)}$	SDOUT output data valid time	DS = 1.0x, 30 pF load	-	-	25	ns

1. Max frequency from 48 MHz RF_XTAL_HS clock source.

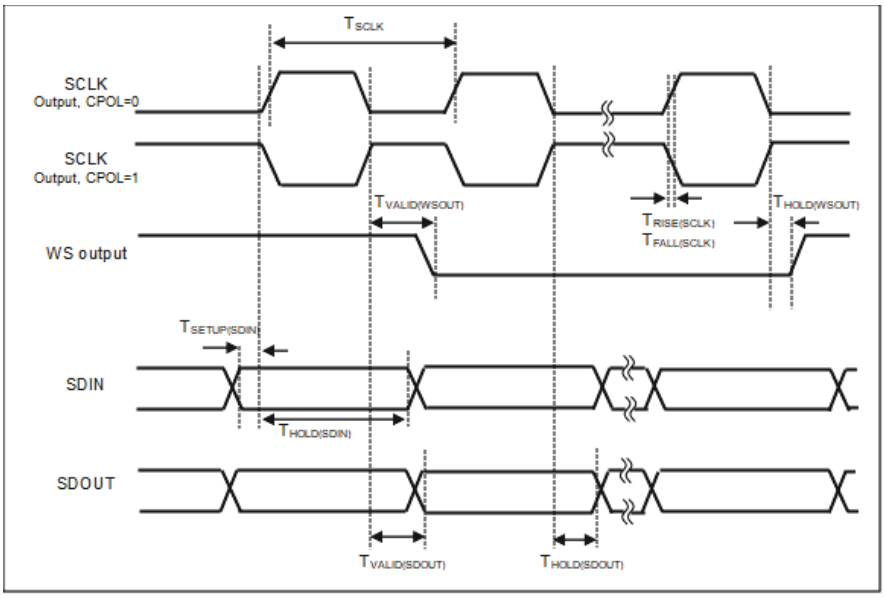


Figure 82. I²S Manager Interface Timing Diagram

30.19.2 PDM Interface

Timing characteristics have been determined by measurements on chip.

Table 69: PDM Interface Timing

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{PDM_CLK} ($1/T_{PDM\_CLK}$)	PDM_CLK frequency range	48 MHz HS XTAL	-	-	12[1]	MHz
$T_{LOW(PDM\_CLK)}$	Clock low time	DS = 0.1x, 15pF load	$0.4/F_{PDM\_CLK}$	-	$0.6/F_{PDM\_CLK}$	s
$T_{HIGH(PDM\_CLK)}$[2]	Clock high time	DS = 0.1x, 15pF load	$0.4/F_{PDM\_CLK}$	-	$0.6/F_{PDM\_CLK}$	s
$T_{RISE(PDM\_CLK)}$	Clock rise time	DS = 0.1x, 15pF load	-	2	-	ns
$T_{FALL(PDM\_CLK)}$	Clock fall time	DS = 0.1x, 15pF load	-	2	-	ns
$T_{SETUP(PDM\_DAT)}$	PDM input data setup time		25	-	-	ns
$T_{HOLD(PDM\_DAT)}$	PDM input data hold time		0	-	-	ns

1. Max frequency from 48 MHz RF_XTAL_HS clock source.
2. The duty cycle range of the generated PDM clock is dependent on the divider setting of MCLKDIV. Even divide ratios generate approximately 50% duty cycle while odd divide ratios generate duty cycles as low as 33%.

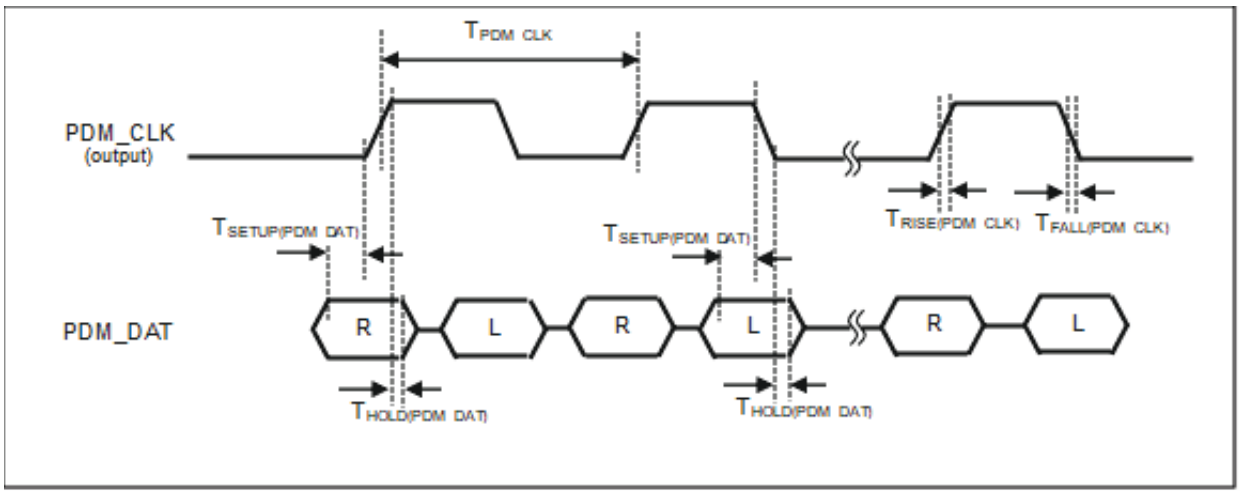


Figure 83. PDM Interface Timing Diagram

31. Ordering Information

Table 70: Ordering Information for Apollo510 Lite Series SoCs

Device Name	Commercial Temp Range (-20°C to 70°C)	Industrial Temp Range (-40°C to 85°C)	Package Type	GPIOs	NVM (MRAM)[1]	SRAM (SSRAM and TCM)	Connectivity	Package[2] Size (mm)
Apollo510 Lite	AP510NLA-CCR	-	CSP	68	2 MB	2 MB	No Connectivity	4.047 x 3.948 x 0.510(max) 110-pin
Apollo510 Lite	AP510NLA-CBR	-	BGA	120	2 MB	2 MB	No Connectivity	5.3 x 5.3 x 0.8(max) 169-pin
Apollo510B Lite	-	AP510BLA-ICR	CSP	68	2 MB	2 MB	BLE 5.4	4.047 x 3.948 x 0.510(max) 110-pin
Apollo510D Lite	AP510DLA-CCR	-	CSP	68	2 MB	2 MB	BLE 5.4, BT Classic	4.047 x 3.948 x 0.510(max) 110-pin
Apollo510D Lite	AP510DLA-CBR	AP510DLA-IBR	BGA	120	2 MB	2 MB	BLE 5.4, BT Classic	5.3 x 5.3 x 0.8(max) 169-pin

1. Factory-installed Cortex-M4 firmware reduces the amount of available NVM which varies for each series derivative. The amount of NVM used for each derivative can be viewed in the Cortex-M55 Memory Map
2. Packing: Tape and Reel

32. Document Revision History

Table 71: Document Revision List

Revision	Date	Description
0.3.0	June 2025	Initial NDA release
0.4.0	November 2025	Front Page Feature List, SoC Product Introduction, Electricals (Recommended Operating Conditions - External Voltage Supplies): - Operating voltage (and applicable voltage rails) upper limit reduced from 3.3 V to 2.2 V. Memory SS: - Added note that MSPI clock on MSPIn_4 configuration is not supported by the Boot ROM. System Power Management: - Added sub-section “Guidance for HP mode usage”. CLKGEN: - Note added that external load capacitors are required to tune the XTAL oscillator circuit GPIO: - “High-Speed Pads” sub-section added to “Functional Overview”. - “GPIO Interrupts” and “Pad Configuration Functions” sections updated; IO Voltage supply for GPIO previously shown powered by VDDH now VDDH2. MSPI: - Clarified MSPI2 limitations on WLCSP package. - Added note that MSPI does not support full duplex operation. IOM: - Added note that IOM does not support full duplex operation. I3C: - “I3C PHY - Transmitter and Receiver” feature added to Functional Overview IOSFD: - Support for I2C operation deprecated. - Corrected “Features” list to state that IOSFD0 is used for half duplex operation. - Updated sections describing DMA transfers. VREG: - Updated “Block Diagram for Voltage Supplies and Regulation” Electrical Characteristics: - Removed option to power the VDDRF_TRX from an external regulator in the External Voltage Supplies table. - Updated Notes column for VDDHx supplies in the External Voltage Supplies table. - Updated VDD18 leakage current spec. - VDDUSB33 bypass capacitor corrected in “USB Power Options” diagrams. - Bypass/high frequency filtering capacitor information for VDDRF_H, VDDRF_PAH and VDDRF_TRX supplies added in Recommended Bypass Capacitors for External Supplies table. - Corrected voltage rating for SIMO Buck bypass capacitors in the “smaller package” option. - $C_{EXT\_XT\_LOAD}$ updated in Low-Frequency Crystal Oscillator table. - I3C section added.

Table 71: Document Revision List

Revision	Date	Description
0.9.0	July 2026	Front Page Feature List, SoC Product Introduction: - Updated high-level and detailed block diagrams - Updated RF's max Tx power and Rx sensitivity Memory Subsystem: - Corrected offsets in PUF System Side Function Descriptions STIMER: - Updated Functional Overview section. MSPI: - Updated MSPI Pin Muxing Tables for CE1 pins in serial, dual and quad data widths. IOM: - Updated maximum transfer sizes for I2C operations to 4095 bytes. I3C: - Removed mention of the deprecated HDR-DDR messaging mode. Voltage Regulator: - Removed mention of the deprecated LDO Mode (no SIMO Buck). Electricals: - External Voltage Supplies: Added note for VDDH3 that it must not be lower than 1.71 V if powering an MSPI instance. - USB Supplies: Updated supply connections on WLCSP when not using USB. - Current Consumption, Display Controller, MSPI, IOM, IOSFD, SDIO, PDM and I2S sections added. - High-Speed Crystal Oscillator specifications updated. - BLE specifications added. - GPADC specifications added. - UART: Max baud rate specification updated.

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